A Subthreshold Analysis of Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs

A dissertation submitted in partial fulfilment of

the requirement for the degree of

Masters of Technology in

VLSI and Embedded Systems

by

Abirmoya A. Santra (211EC2075)

to the

Department of Electronics and Communication Engineering
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CERTIFICATE

This is to certify that the thesis entitled "*A sub-threshold analysis of Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs*" being submitted by Abirmoya Santra bearing *roll no. 211EC2075* to the National Institute of Technology, Rourkela, in the Electronics and Communication Engineering Department is a bonafide work carried out by him under my supervision and guidance. The research reports and the results presented in this dissertation have not been submitted in parts or in full to any other University or Institute.

Place: Rourkela

Date: 24 May, 2013

Prof. (Dr.) P. K. TIWARI
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Dedicated to my country and my people.

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Abirmoya A. Santra

ABSTRACT

With the technological leap to another milestone in sub 20nm regime, the conventional FETs seems to be of little use in continuing scaling with the least short channel effects (SCEs). Hence, non-conventional devices had to intervene in the rescue of the ITRS. Where the devices with the silicon-on-insulator substrates, strain, double gate, finned gate, omega and pi gates upheld the Moore's law, the Gate-All-Around (GAA) emerged to be the ultimate solution. To further improve the sub threshold electrical parameters, a multi material gate may be inserted as the gate material.

Thus, extending the idea of a triple material gate in the cylindrical GAA (CGAA) MOSFET, a TM-CGAA is obtained with better SCE characteristics. In this work, an accurate analytical sub threshold models has been developed for an undoped tri-material cylindrical gate-all-around (TM-CGAA) MOSFET considering parabolic approximation of the channel. The centre (axial) as well as the surface potential model is obtained by solving the 2-D Poisson's equation in the cylindrical co-ordinates. The work refutes the estimation of the characteristic length using surface potential as in the previous work and proposes the use of centre potential based characteristic length formulation for an accurate analysis.

The developed centre potential model is used further to develop the threshold voltage model and also extract DIBL from the same. The centre potential model was further applied to estimate the sub threshold drain current and the sub threshold swing of the device. An extensive analysis of the device parameters like the cylinder diameter, oxide thickness, gate length ratio, etc. on the sub threshold electrical parameters is demonstrated. This gives a highly accurate model which closely matches with the simulations. The models are verified by the simulations obtained from 3-D numerical device simulator Sentaurus from Synopsys.

To sum up, the work includes development of the sub threshold analytical models, simulation and verification of the developed model of TM-CGAA MOSFET.

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List of Acronyms

BOX: Buried Oxide

CGAA: Cylindrical Gate-All-Around

CMOS: Complementary Metal Oxide Semiconductor

DIBL: Drain Induced Barrier Lowering

HCE: Hot Carrier Effect

IGFET: Insulated Gate Field Effect Transistor

ITRS: International Technology Roadmap for Semiconductor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

NWFET: Nano Wire Field Effect Transistor

SCE: Short Channel Effect

SOI: Silicon-on-Insulator

TCAD: Technology Computer-Aided-Design

TM-CGAA: Triple Metal Gate Cylindrical Gate-All-Around

UFET: Ultra Thin Field Effect Transistor

VLSI : Very Large Scale Integration

List of Symbols

Gate Oxide Thickness	t_{ox}
Silicon layer Thickness	t_{Si}
Gate Length	$L = L_1 + L_2 + L_3$
Control Gate Length	L_1
Screen Gate Lengths	L_2 , L_3
Work function of Control Gate	φ_{M1}
Work functions of Screen Gate	φ_{M2} , φ_{M3}
Control Gate Potential	$\phi_1(x, y)$
Screen Gate Potential	$\phi_2(x, y), \phi_3(x, y)$
Centre Potential	$\phi_c(x)$
Surface Potential	$\phi_s(x)$
Source and Drain Doping	N_d
Channel Doping	N_a
Mobility	μ_n
Gate to Source Voltage	V_{GS}
Drain to Source Voltage	V_{DS}
Threshold Voltage	V_{th}
Drain Current	I_{ds}
Subthreshold Swing	S_t

Chapter 1

INTRODUCTION

1.1 Scaling: A Historical Perspective

The twentieth century marked the beginning of an era in industrial electronics, automation, information sharing and technology. Communication technology multiplied in leaps and bounds. In no point in human history, the human race was ever been connected as it is today. Miniaturization of computer and hand held gadgets with every possible applications; be it audio, video, high speed communication; revolutionized the world of interconnectivity and entertainment. It's all attributed to the high speed ultra small sized, low power semiconductor devices, sensors, all new materials and their implementation through VLSI design.

It all begins with the perception of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to replace the vacuum tube technology with small sized semiconductor transistor technology [1]. The first practical demonstration took place in 1960 by Kahng and Atilla [2] in the form of the Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In 1958, Jack Kilby at Texes Instruments conceived the idea of the Integrated Circuits (IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC (a S-R flip flop) as shown in Fig. 1 [3]. It then came in 1959 when Richard Feynman delivered his notable speech, "There is plenty of room at the bottom", acknowledging the high performance achievement of the materials at the reduced dimensions [4]. Another visionary prophecy from Gordon Moore, then with Fairchild Corp. and co-founder of Intel, states that, "The number of transistors on integrated circuits doubles approximately every two years". This prophecy has been accurate for more than 3 decades as shown in Fig. 2. The year 1962 saw the growth of the first logic family, the TTL [3]. Intel introduced the first

microprocessor in 1972 which used more than 2000 PMOS transistors. Following the Moore's law the transistor count increased exponentially [3]. Then next few microprocessors used the NMOS technology which was routed out soon due to heavy dynamic power consumption with the increased number of transistor per chip. Then with the advent of the CMOS technology which consumed the least power, scaling technology sailed from the small scale integration (SSI) to Very Large Scale Integration (VLSI) and now spearheading towards the nanotechnology.

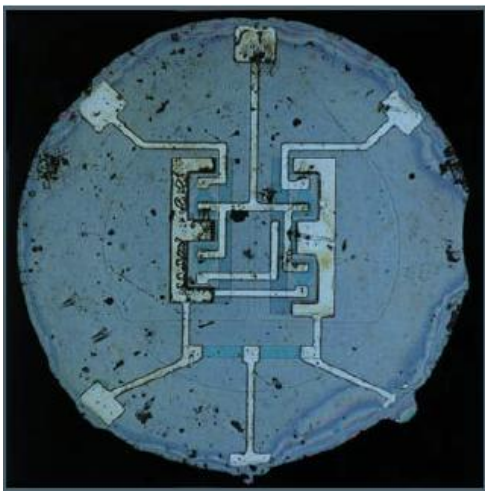


Fig. 0.1 First IC fabricated by Jay Last's development group at Fairchild Corp. **[4]**

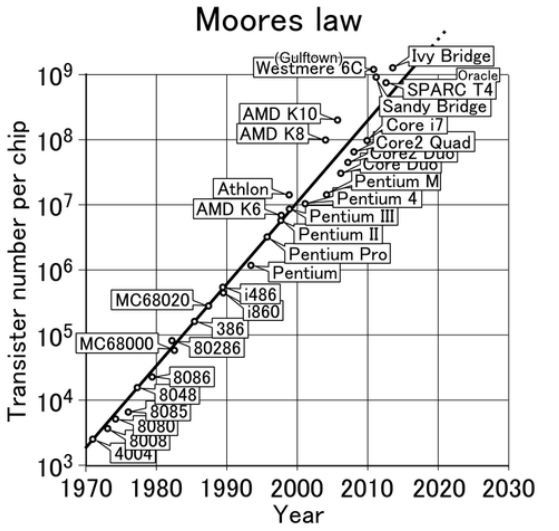


Fig. 0.2 Transistor Integration on Chip displaying Moore's Law. **[5]**

Another basic advantage that CMOS technology provides is the presence of definite scaling laws. The International Technology Roadmap for Semiconductor (ITRS) has laid a roadmap to direct this scaling in terms of power consumption and cost incurred. As evident from the ITRS 2010 in Fig. 3, the year 2013 with technology node 22nm is project to have physical channel length of 10nm and less. The latest Itanium-7 quad core GPU processor contains more 1.1 billion transistors in a 160 mm² chip area and Intel 32 nm SRAM wafer (1 Tb) has about 800 billion transistors [6]. Device engineers throughout the world have made this wonder come true through a magic named "Scaling". Scaling is defined as controlled modification of the device dimensions such that it acquires lesser chip area while maintaining

the long channel characteristic and performance. Dennarad and fellow workers proposed the scaling approach in 1972 [7].Scaling not only reduces the device dimensions rendering to a higher packing density but it also leads to significant dynamic power saving through lesser voltages. The scaling approach stated that both the lateral and vertical dimensions of the transistor should be scaled by the same scaling factor in order to avoid the SCEs and ensure good electrostatic control when fabricating the smaller devices, and by the same scaling factor, the supply voltage should be reduced and substrate doping concentration should be increased.

Today's monolithic Integrated Circuits (ICs) use the MOSFET as a basic switching element for digital logic applications and as an amplifier for analog applications. This has resulted in chips that are significantly faster and have greater complexity in every generation while continually bringing down the cost per transistor.

1.2 Scaling Problems

Integration of billions of transistors on a chip has been possible due to the possibility to pattern every smaller feature on silicon through optical lithography. As optical lithography enters the sub-wavelength regime, light diffraction and interference from sub wavelength pattern feature causes image disorder. Therefore, patterning becomes difficult without adopting resolution enhancement techniques.

The ITRS's most recent projection provides some insight as to current market drivers. Fig. 4 illustrates that the power consumption trend versus power requirements is creating the "Power Gap" akin to the "Design Gap" that the industry dealt with a decade ago. This gap is creating a need to manage power at all levels of abstraction and majorly at the device level.

The power consumption is approximated by [8]

$$P_{diss} = P_D + P_S = \alpha f C_L V_{DD}^2 + V_{DD}\left(I_{leakage} + I_{th} 10^{-\frac{V_{th}}{s}} \right) \quad (0.1)$$

where P_D is the dynamic power dissipation, P_S is the static power dissipation, α is the activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, $I_{leakage}$ is the total leakage current, I_{th} is the threshold current, V_{th} is the threshold voltage and s is the subthreshold swing. The power consumption is lowered through lower V_{DD}, $I_{leakage}$ and s; and higher V_{th}.

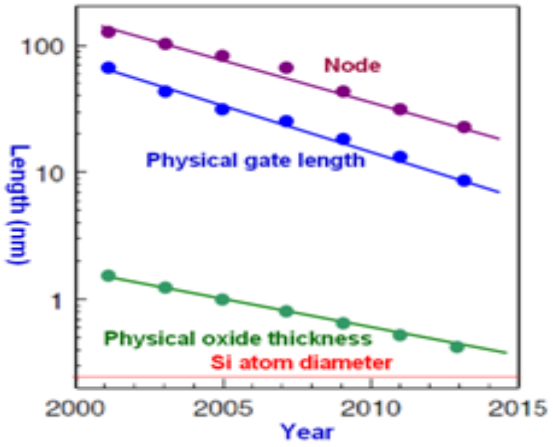


Fig. 0.3. Shrinking gate length with of scaling. years (Courtesy: ITRS 2010)

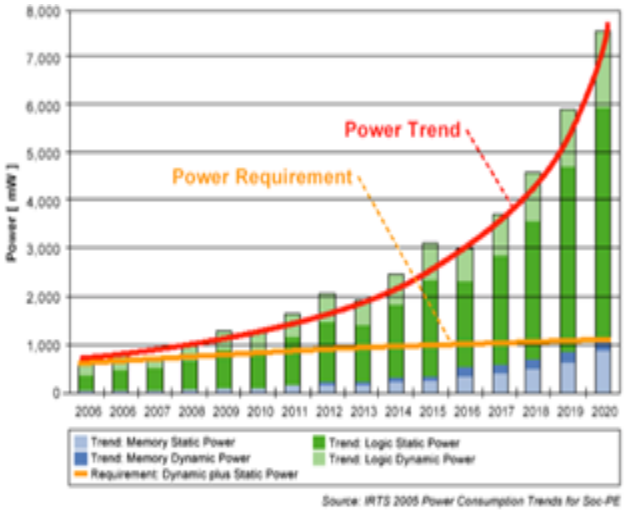


Fig. 0.4. Power Consumption trends with years of scaling. (Courtesy: ITRS 2005)

Thus V_{DD} and V_{th} are in conflict for which the gate oxide needs to be scaled tremendously which in turn increases gate tunnelling leakages. Also, higher substrate doping is must to check the short channel effects (SCEs) but again this diminishes the current drive due to

increased scattering. To trade-off between the power consumption, SCE and the lower current, is the need of the hour which the conventional MOSFETs fails to achieve. This gives way to creation of alternative device structures and architectures to continue further CMOS scaling.

Let's have a physical insight into the problems due to scaling. MOSFET scaling alters both lateral and vertical device dimensions.

1.2.1 *Vertical Scaling*

1.2.1.1. *Polysilicon Depletion Effect*

With vertical scaling, the effective oxide thickness increases, resulting in the degradation of the gate capacitance and transconductance. One of the factor responsible for this is scaling of the oxide whereas the other being thick polysilicon depletion layer when the device is operated at inversion. This depletion region cannot be further reduced due to doping limitations due to the solid solubility of silicon (~10^{19}-10^{20} cm^{-3}). The effect also leads to a threshold voltage shift, which gets more pronounced at low polysilicon gate doping densities. Thus, the technology node predicts the use of metal gates to avoid this challenge.

1.2.1.2. *Quantum effects*

Scaling the oxide leads to strong surface electric field near the silicon/oxide interface creating a potential well and leading to quantum confinement of the inversion carriers, giving rise to discrete sub-bands for motion in the direction perpendicular to the interface and shifting the peak of the inversion charge centroid away from the interface. At inversion, the peak of the inversion carrier concentration peak is located around 1.2 nm away from interface in silicon. The confinement decreases the inversion charge density at a given bias, increases the effective oxide thickness and increases the threshold voltage.

1.2.1.3. *Gate Tunnelling*

With the diminishing gate oxide thickness, static power dissipation increases and the major contributor is the Gate Tunnelling. The tunnelling may take place through mechanisms like the direct tunnelling or the Fowler Nordheim tunnelling. Use of high-k dielectric materials (viz. HfO_2, $HfSiO_4$, and Si_3N_4) are employed to check gate tunnelling.

1.2.2 *Lateral Scaling*

1.2.2.1. *Threshold voltage roll-off and DIBL*

As the lateral dimensions are scaled, the S/D channel p-n junction depletion width becomes significant in comparison to the channel length leading to loss of gate control over the channel. The channel barrier reduces tremendously with increasing scaled channel which is manifested as threshold voltage roll off or a sharp fall of the threshold voltage with a scaled channel length.

The V_{th} roll-off is more dramatic when the drain bias is high. This is expected, since an increase in drain voltage leads to further penetration of the drain-induced field into the channel of the transistor, reducing the lateral potential barrier that is typically controlled by the gate. This effect is termed drain induced barrier lowering (DIBL). Vth lowering due to DIBL can be qualitatively explained by a semi-empirical 'charge sharing' model which considers the splitting of the depletion charge under the gate into two parts – one controlled by the gate, the other controlled by the source and drain. This introduces a correction of the maximum depletion charge controlled by the gate which determines the threshold voltage.

$$V_{th} = V_{FB} + 2\phi_f - \frac{Q'_d}{C_{ox}} \tag{2}$$

where, $Q'_d = Q_d - \Delta Q$ (3)

$Q'_d, Q_d \Delta Q$ represents the depletion charge under gate control, the total depletion charge and depletion charge under drain control.

1.2.2.2. *Hot Carrier Effect*

Hot-carrier (HC) degradation affects reliability, increases SCE and causes long-term instability, manifested by a threshold voltage decrease and sub-threshold drive current increase. The high electric field near the drain creates hot carriers which are injected into the oxide with enough energy to create defect states (traps) in the oxide near the silicon/oxide interface. It is found that only hot electrons having energy of 0.6eV larger than the Si-SiO2 conduction band discontinuity can cause SiO_2 degradation in n-channel MOSFETs. The degradation is attributed to the breaking of the ≡SiH bond at the interface.

1.2.2.3. *Mobility Degradation*

Following the rules of scaling, for a planar bulk MOSFET, continuous scaling requires continuous increase in the channel doping (N_a). This is because it is desired to have a lower junction electric field in the channel region. Also higher doping ensures non-overlap of the source and drain depletion in the channel. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel.

1.3 Technology Boosters: Solution to Scaling

1.3.1 *Channel Engineering Techniques*

1.3.1.1. *Shallow S/D Junction*

Lowering the source/drain junction depths (especially near the gate edge, where the source/drain regions are called ‘extensions’) reduces the drain coupling to the source barrier. However, as the source/drain junction depths get shallow, their doping must be increased so as to keep the sheet resistance constant. Solid solubility of dopants puts an upper limit (~10^{20} cm^{-3}) on the doping density. Therefore, further reduction in 13 junction depth causes an increase in the series resistance encountered in accessing the channel. Also, from a

technological point of view, it becomes difficult to form ultra shallow junctions that remain abrupt after the annealing steps needed to activate the dopants and achieve low resistivity [8]. The formation of abrupt S-D junctions also leads to an increase in the band-to-band tunneling leakage component. All these factors degrade the overall transistor performance.

1.3.1.2. *Halo Doping*

To overcome the SCEs, various channel engineering techniques like double-halo (DH) and single-halo (SH) or lateral asymmetric channel (LAC) devices have been proposed. In the subthreshold region, although the halo doping is found to improve the device performance parameters for analog applications (such as gm/Id, output resistance and intrinsic gain) in general, the improvement is significant in the LAC devices. Halo doping led to a higher drive current in the saturation region. The halo device pinch–off region occurs in the halo implant region, since that region is closest to the drain and has a threshold voltage higher than the uniformly doped region.

1.3.1.3. *Strain*

To maintain a lower junction electric field in the channel and non-overlap of the source and drain depletion in the channel, doping becomes imperative. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel. The mobility of the charge carriers is enhanced through a concept known as the strain technology. To sum it all the benefits of strain, it results in a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility. By increasing the Ge concentration of the relaxed $Si_{1-X}Ge_X$ substrate, the amount of biaxial strain and therefore

higher magnitude of the mobility enhancement can be achieved. Literature had confirmed a mobility enhancement factor of 2.3 for a 30% Ge concentration.

1.3.1.4. *Multi-Material Gate*

One of the prominent means to get rid of hot carrier effect (HCE) is using cascaded gate structure consisting of two or more metals of different work functions. This structure is commonly known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long *et al.* [9] or Triple-Material-Gate (TMG) in 2008 proposed by Razavi *et al*. [10]. The metal gates are so cascaded that the gate near the drain is a metal (M_2) with lower work-function and the source side metal (M_1) is of relatively higher workfunction. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency. Li Jin *et al.* described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [11]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations. The metal gate M_2 is thus rightfully known as the *Screen Gate* (L_2) and the metal M_1 as the *Control Gate* (L_1).

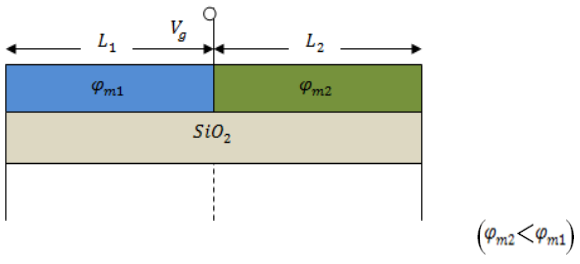


Fig. 0.5 The dual metal gate structure

1.3.2 *Gate Engineering Techniques*

1.3.2.1. *High-k dielectric*

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45 nm CMOS technology generation. This is the first time that traditional oxides or oxynitrides have been replaced in gate stacks, to enable continuous scaling of the EOT.

1.3.2.2. *Metal Gate*

Initially, poly-Si/high-k combination gate stack was considered as a route to improving gate leakage. However theoretical studies and experimental data show mobility degradation compared to the use of metal gates. Depending on the gate dielectric, the work function varies due to differing band alignments.

1.3.2.3. *Multiple Gate*

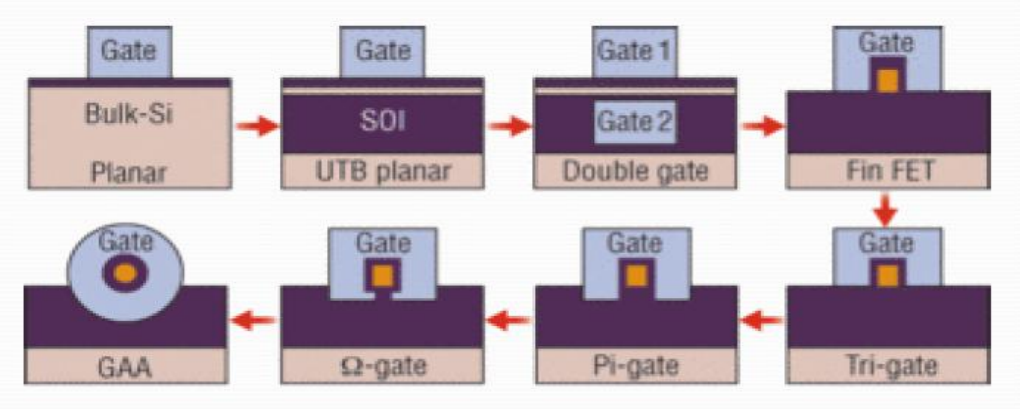


Fig. 0.6. Progress of the MOSFET Technology through multiple-gates [5]

A potential candidate to continue the MOSFET scaling further is the fully-depleted silicon-on-insulator (FDSOI) MOSFET. Rigorous research of the FD SOI MOSFETs revels that this transistor possesses higher transconductance, lower threshold voltage roll-off and steeper subthreshold slope compare to the bulk MOSFET. In the FDSOI MOSFETs, the front gate parasitic junction (source/drain to channel) capacitances reduces resulting in higher switching speeds. The presence of the buried oxide (BOX) further removes drawbacks like leakage current, threshold voltage roll off, higher sub-threshold slopeand body effect. However, due to the ultra thin source and drain regions, FD SOI MOSFETs possess large

series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. To prevent the encroachment of electric field lines from the drain on the channel region, special gate structures can be used as shown in Fig. 16. Such "multiple"-gate devices include double-gate transistors, triple-gate devices such as the quantum wire, the FinFET and Δ-channel SOI MOSFET, and quadruple-gate devices such as the gate-all-around device, the DELTA transistor, and vertical pillar MOSFETs [12]. In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach, however, has the inconvenience of increased junction capacitance and body effect. A much more efficient device configuration is obtained by using the double-gate transistor structure. Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion or volume accumulation in the thin layer (for enhancement- and depletion-type devices, respectively), leading to an increase of the number and the mobility of electrons and holes as well as driving current (additional gain in performance in a loaded environment), optimum subthreshold swing and the best control of short channel effects and off-state current, which is the main challenge for future nanodevices due to the power consumption crisis and the need to develop green/sustainable ICs.

The triple-gate MOSFETs have made the advent of 22nm technology node feasible at industrial scale in 2011 [13, 14, 15]. One among various multi-gate structures, triple-gate MOSFET enjoys the silicon channel engaged from three sides giving enhanced on-current and reduced off-current. As the MOS dimension has attained its physical limit, the scaling beyond 22nm node is thus an insuperable task. The improvement in device performance, however, are believed to be continued in the company of multi-gate MOSFETs as they

employ third dimension offering superb gate control over channel from several sides. The degree of gate controllability increases further with the quadruple-gate, the Omega/Pi-gate and the gate-all-around (GAA) structures respectively with better combinations of performance and energy efficiency [12]. As far as the characteristics lengths of the device structures are concerned, the gate-all-around MOSFETs offer the lowest characteristic length and hence the highest capability to be scaled for a given gate oxide thickness [16]. This capability gets coupled with the highest current drive per unit silicon area and demonstrates strong confinement of the electric field owing to the gate surrounding the channel.

1.4 Thesis Organization

Following the introduction, the rest of the dissertation is organized as follows:

Chapter 2: The chapter presents an extensive literature review on the cylindrical Gate-All-Around MOSFET. Finally it arrives at the problem statement of the current work.

Chapter 3: This chapter describes the complete details of two dimensional (3D) Sentaurus device simulator form Synopsys to describe the model

Chapter 4: This chapter reports the surface potential and the threshold voltage model.

Chapter 5: This chapter reports the sub-threshold current and the sub-threshold swing model.

Chapter 6: This chapter will conclude on the results from all the simulations. Discussions and analysis are included in this section. There is, also, a discussion on the suggestion for future work.

CHAPTER 2
LITERATURE REVIEW

2.1. Fabrication

To maintain a very low off-state current and boost the driving current, 3-D integration of CGAA is a promising solution. Using SON process, three stacked GAA sub-15 nm nanowires, with 100 nm length and 1.8 nm EOT (high k/metal gate stack) has shown extremely high driving current and very low leakage currents (Ion/Ioff: 6.5 mA/lm to 27 nA/lm for nMOS—I_{on}/I_{off}: 3.3 mA/lm-0.5 nA/lm for pMOS). A new optional independent gate nanowire with a FinFET-like structure named UFET has also been reported, leading to new design flexibility. These 3D structures can be extended to a combined vertical and lateral integration for logic, memories and NEMS applications (Fig. 11). The 3D-NWFET and UFET, compared to a co-processed FinFET, relaxes the channel width requirement for a targeted DIBL and improves transport properties (Fig. 12). UFET also exhibits significant performance boosts compared to Independent-Gate FinFET (IG-FinFET): a two-decade smaller Ioff current and a lower subthreshold slope (82 mV/dec. instead of 95 mV/dec.). This highlights the better scalability of 3D-NWFET and UFET compared to FinFET and IG-FinFET [16].

In 2013, Deyuan Xiao and Xi Wang patented the CMOS fabrication procedure using Gate-all-around CMOSFET devices. This shows the feasibility of fabricating the device.

2.2. CGAA: Past Works

Due to the interest in this device for future CMOS technology, simple compact models will be needed for implementing in electrical circuit simulators. In an attempt to model the device characteristics of GAA MOSFETs, El Hamid *et al*. [17] showed the first analysis of a cylindrical GAA MOSFET with an undoped channel in 2007, and reported the occurrence of

inversion at the body centre rather than the surface. The electric field density, however, in the CGAA MOSFETs increases tremendously with scaling in the axial direction resulting in the formation of highly energetic and accelerated "hot carriers" [18, 19]. These hot carriers, under the influence of the transverse field, gains sufficient energy to collide with the oxide and damage the interface, and gets trapped in the oxide region. Researchers like Yu *et al.* [20] and Te-Kuang [21] have analysed the damaged CGAA MOSFETs using a two-dimensional (2D) analytical model through a parabolic potential approximation with and without an effective conducting path effect respectively. An efficient means to get rid of such hot carrier effects (HCEs) lies in gate engineering by cascading two or three different metal gates. In a dual metal gate, GAA has a single step variation in the potential profile effective in curbing HCE and DIBL. Chiang [22] showed a subthreshold behavior analysis of undoped CGAA using 2-D analytical model assuming surface potential inversion. Then came the triple-material-gate (TMG) structure having one control gate and two screen gates near source and drain ends respectively. The two steps in the potential profile, owing to difference in work functions of the metals, results in increased lateral field allowing the carriers to travel faster thereby improving the gate transport efficiency. The higher immunity of the minimum potential point of the structure to the DIBL and HCEs induced Wang *et al.* to propose a threshold voltage model of triple-material gate-all-around (TM-CGAA) MOSFETs [23]. The channel potential was derived at the surface by solving the 1-D Poisson's and 2-D Laplace's equations in three separate regions using evanescent mode analysis. Although the analysis rendered some fruitful results, the cumbersome mathematical expressions failed to predict the characteristic length precisely. Further, in [23], a moderately doped channel is considered while threshold voltage is formulated by utilizing the classical definition of the threshold voltage. It should be noted that for a moderately doped CGAA MOSFET, channel centre will be inverted more than

channel surface as supported by the simulation results from Fig. 2.2 and hence classical definition of threshold voltage may not be valid.

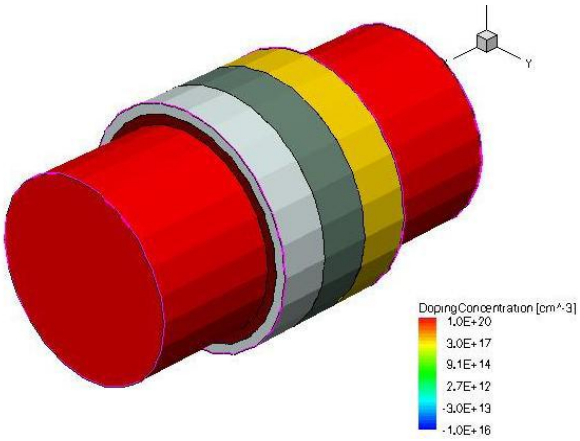


Fig. 0.1. The simulated structure in Sentaurus

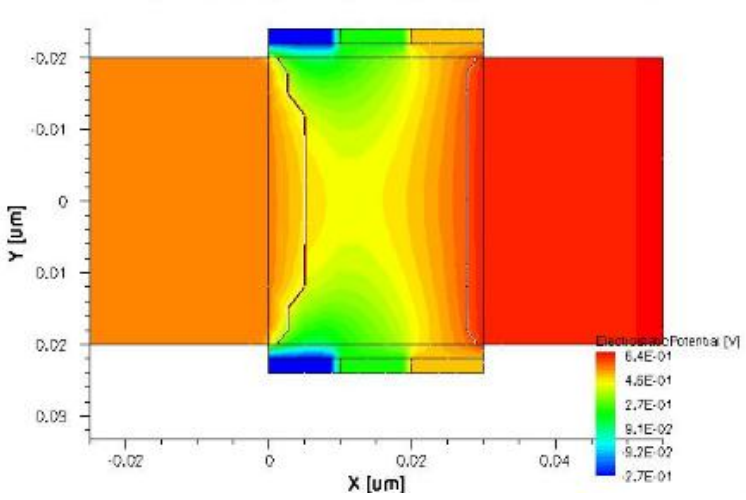


Fig. 0.2. Cross-section of the 2-D Potential distribution of TM-CGAA obtained by Sentaurus

In the present work, it has been demonstrated that the channel forms at the Si body center first than at the surface. Thus, formulation centre potential is more worthy than the surface potential. The natural length derived through centre potential will be more accurate than that at surface. A rather simplified method has been adopted to derive the device characteristics employing parabolic potential approximation in the channel. The derived center potential

model has been further utilized to find the threshold voltage expression. Besides this, the drain induced barrier lowering (DIBL) is also evaluated from the model. Though the accuracy of the model is checked upto 20nm of channel length, however the model is capable to take on the device characteristics beyond 20nm gate length. The model results are verified with the simulation results obtained from the numerical device simulator Sentaurus from Synopsis [24].

2.3. Device Structure

The cross sectional diagram of the fully depleted TM-GAA MOSFET structure used for modeling and simulation is shown is shown in Fig. 1. The radial and lateral directions are assumed to be along the radius and the z- axis of the cylinder as shown in the Fig. 1. The surrounding metals divide the entire channel region into three regions named as region I, II and III as shown in Fig. 1. The lengths of the three regions connected in a non-overlapping way are symbolized as L_1, L_2 and L_3. The device has uniformly doped source/drain with doping density of $N_D = 1\times10^{20} cm^{-3}$. The channel is kept lightly doped with doping density of $N_A = 1\times10^{16} cm^{-3}$. The gate oxide thickness and the diameter of the silicon pillar are t_{ox} = 2nm and t_{Si} =40 nm respectively. The work function of the gate materials in decreasing order from source to drain are: φ_{M1} = 4.8eV (e.g., Au), gate material 2 with φ_{M2} = 4.6 eV (e.g., Mo), and gate material 3 with φ_{M3} = 4.4 eV (e.g., Ti).

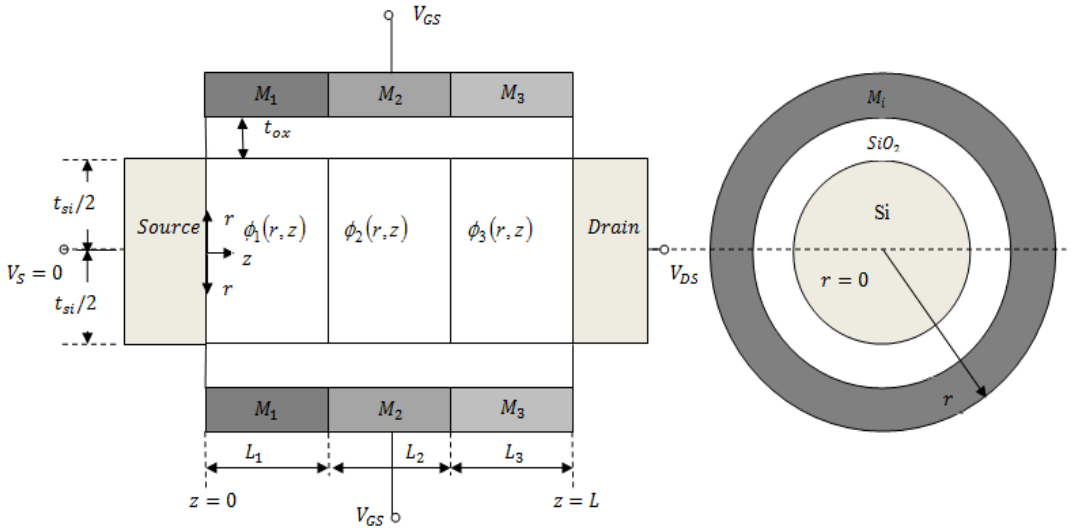


Fig. 0.3 Cross sectional view and side-view of the TM-GAA MOSFET

2.4. Research Problem Statement

In this dissertation, novel features offered by the introduction of a Dual-Material Gate (DMG) in fully depleted silicon-on-insulator are studied by means of two-dimensional analytical modeling and numerical simulation studies. This is accomplished in terms of the following intermediate stages:

i) Demonstrate the inversion at the body centre through analytical potential model. Thereby, calculate the accurate natural length of the TM-CGAA.

ii) A physics based 2-D analytical model for the centre/ surface potential distribution in the TM-CGAA MOSFET is developed and verified against numerical simulation results.

ii) Threshold voltage and DIBL model for a fully-depleted TM-CGAA is developed based on the centre potential model to show the efficacy of the TMG structure in suppressing short-channel effects.

iii) Two-dimensional subthreshold current and subthreshold swing model numerical simulation studies are used to investigate and compare the benefits of SCEs.

Chapter 3

SENTAURUS: 3D SIMULATOR

3.1. SENTAURUS: An Introduction

Sentaurus Device simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms. A real semiconductor device, such as a transistor, is represented in the simulator as a 'virtual' device whose physical properties are discretized onto a nonuniform 'grid' (or 'mesh') of nodes.

Therefore, a virtual device is an approximation of a real device. Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space. The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation. Each virtual device structure is described in the Synopsys TCAD tool suite by a TDR file containing the following information:

- The grid (or geometry) of the device contains a description of the various regions, that is, boundaries, material types, and the locations of any electrical contacts. It also contains the locations of all the discrete nodes and their connectivity.
- The data fields contain the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes. By default, a device simulated in 2D is assumed to have a 'thickness' in the third dimension of 1 μm.

3.2. Tool Flow

In a typical device tool flow, the creation of a device structure by process simulation (Sentaurus Process) is followed by remeshing using Sentaurus Structure Editor or Mesh. In this scheme, control of mesh refinement is handled automatically through the file `_dvs.cmd`. Sentaurus Device is used to simulate the electrical characteristics of the device. Finally, Tecplot SV is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics.

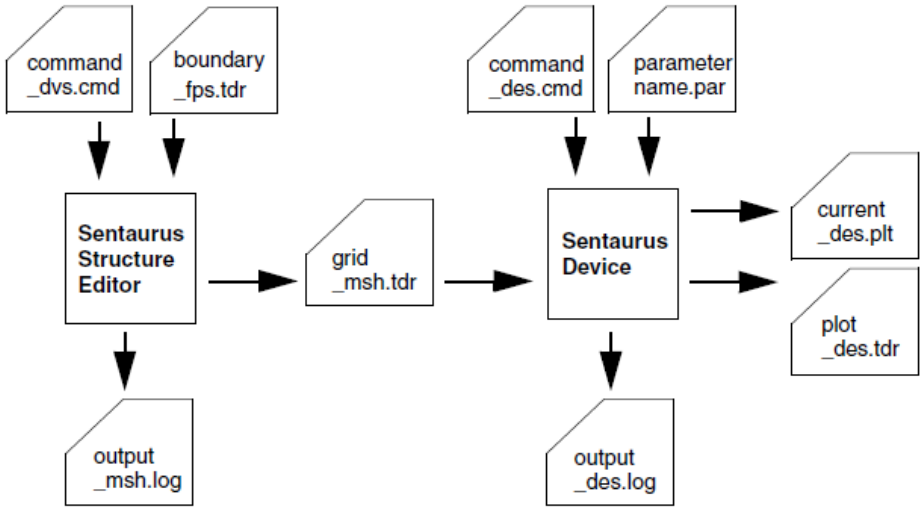


Fig. 0.1. Typical tool flow with device simulation using Sentaurus Device

3.3. Typical flow of Sentaurus Device Simulator

An example of a complete command file (`tm_1:1:1_60nm`_des.cmd in the Sentaurus Workbench project simple Id-Vg) is presented. Each statement section is explained individually.

```
File {* input files:

Grid= "tm_1:1:1_60nm_msh.tdr"
* output files:
Plot
= "tm_1:1:1_60nm_vds_0.1_des.tdr"
Current = "tm_1:1:1_60nm_vds_0.1_des.plt"
Output = "tm_1:1:1_60nm_vds_0.1_des.log"
}
```

```
Electrode {
{ Name="source" Voltage=0.0 }
{ Name="drain"
Voltage=0.1 }
{ Name="gate" Voltage=-0.4
}
}
Physics {
Fermi
Mobility (DopingDependence HighFieldSat Enormal(Lombardi))
Recombination(SRH(DopingDependence))
EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
}
Plot {
eDensity hDensity eCurrent hCurrent
Potential SpaceCharge ElectricField
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
}
Math {
-CheckUndefinedModels
Extrapolate
RelErrControl
}

Solve {
Poisson
Coupled { Poisson Electron }
Quasistationary ( MaxStep=0.1
Goal{ Name="gate" Voltage=1 }
)
{ Coupled { Poisson Electron } }
}
```

The code may be categorized under different sub-sections:

3.3.1. File Section

```
*input files and * output files:
```

These are comment lines.

```
Grid= "tm_1:1:1_60nm_msh.tdr"
```

This essential input file (default extension .tdr) defines the mesh and various regions of the device structure, including contacts. Sentaurus Device automatically determines the dimensionality of the problem from this file. It also contains the doping profiles data for the device structure.

```
Plot= "tm_1:1:1_60nm_vds_0.1_des.tdr"
Current = "tm_1:1:1_60nm_vds_0.1_des.plt"
Output = "tm_1:1:1_60nm_vds_0.1_des.log"
```

This is the file name for the final spatial solution variables on the structure mesh (extension _des.tdr).

3.3.2. Electrode Section

The Electrode section defines all the electrodes to be used in the Sentaurus Device simulation, with their respective boundary conditions and initial biases. Any contacts that are not defined as electrodes are ignored by Sentaurus Device.

```
Name="source", Name="drain", Name="gate",
```

Each electrode is specified by a case-sensitive name that must match exactly an existing contact name in the structure file. Only those contacts that are named in the Electrode section are included in the simulation.

```
Voltage=0.0
```

This defines a voltage boundary condition with an initial value. One or more boundary conditions must be defined for each electrode, and any value given to a boundary condition applies in the initial solution. In this example, the simulation commences with a bias on the drain.

```
Barrier=-0.55
```

This is the metal–semiconductor work function difference or barrier value for a polysilicon electrode that is treated as a metal. This is defined, in general, as the difference between the metal Fermi level in the electrode and the intrinsic Fermi level in the semiconductor. This barrier value is consistent with n+-polysilicon doping.

3.3.3. Physics Section

The Physics section allows a selection of the physical models to be applied in the device simulation. In this example, it is sufficient to include basic mobility models and a definition

of the band gap (and, therefore, the intrinsic carrier concentration). Potentially important effects, such as impact ionization (avalanche breakdown at the drain), are ignored at this stage.

```
Physics {
Fermi
Mobility (DopingDependence HighFieldSat Enormal(Lombardi))
Recombination(SRH(DopingDependence))
EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
}
```

```
Mobility (DopingDependence HighFieldSat Enormal)
```

Mobility models including doping dependence, high-field saturation (velocity saturation), and transverse field dependence are specified for this simulation. HighFieldSaturation can be specified for a specific carrier (for example, eHighFieldSaturation for electrons) and is a function of the effective field experienced by the carrier in its direction of motion.

```
EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
```

This is the silicon bandgap narrowing model that determines the intrinsic carrier concentration.

3.3.4. Plot Section

The Plot section specifies all of the solution variables that are saved in the output plot files (.tdr). Only data that Sentaurus Device is able to compute, based on the selected physics models, is saved to a plot file.

3.3.5. Math Section

Sentaurus Device solves the device equations (which are essentially a set of partial differential equations) self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and Sentaurus Device attempts to converge on a solution that has an acceptably small error.

```
Extrapolate
```

In quasistationary bias ramps, the initial guess for a given step is obtained by extrapolation

from the solutions of the previous two steps (if they exist).

`RelErrControl`
Switches error control during iterations from using internal error parameters to more physically meaningful parameters `(ErrRef)`

3.3.6. Solve Section

The Solve section defines a sequence of solutions to be obtained by the solver. The drain has a fixed initial bias of , and the source and substrate are at To simulate the IdVg characteristic, it is necessary to ramp the gate bias from to and obtain solutions at a number of points in-between. By default, the size of the step between solution points is determined by Sentaurus Device.

`Poisson`

This specifies that the initial solution is of the nonlinear Poisson equation only. Electrodes have initial electrical bias conditions as defined in the Electrode section. In this example, a 100 mV bias is applied to the drain.

```
Coupled {Poisson Electron}
```

The second step introduces the continuity equation for electrons, with the initial bias conditions applied. In this case, the electron current continuity equation is solved fully coupled to the Poisson equation, taking the solution from the previous step as the initial guess. The fully coupled or ‘Newton’ method is fast and converges in most cases. It is rarely necessary to use a ‘Plugin’ (or the so-called Gummel) approach.

```
Quasistationary (Goal { Name="gate" Voltage=2 })
{ Coupled { Poisson Electron } }
}
```

The `Quasistationary` statement specifies that quasi-static or steady state ‘equilibrium’ solutions are to be obtained. A set of `Goals` for one or more electrodes is defined in parentheses. In this case, a sequence of solutions is obtained for increasing gate bias up to

and including the goal of . A fully coupled (Newton) method for the self-consistent solution of the Poisson and electron continuity equations is specified in braces. Each bias step is solved by taking the solution from the previous step as its initial guess. If `Extrapolate` is specified in the `Math` section, the initial guess for each bias step is calculated by extrapolation from the previous two solutions.

3.3.7. List of Parameter Values used in Simualtion

Table 0.1. Parameter List of values used for Simulations

Parameters	**Values**
t_{ox}	2 nm-7 nm
t_{Si}	30 nm- 60 nm
$L_1 : L_2 : L_3$	1:2:3, 1:1:1, 3:2:1
L	20 nm to 200 nm
φ_{M1}	4.8 eV (Au: Gold)
φ_{M2}	4.6 eV (Mo: Molybdenum)
φ_{M3}	4.4 eV (Ti: Titanium)
N_d	10^{20} cm^{-3}
N_a	10^{16} cm^{-3}
μ_n	1076 cm^2/(V-S)
V_{GS}	0-1 V
V_{DS}	0.1-1.1 V

CHAPTER 4
CENTER POTENTIAL AND THRESHOLD VOLTAGE FORMULATION

4.1. Centre Potential

The potential distribution shows no variations with the angular variation in the θ axis. The potential distribution $\phi(r,z)$ in the channel region has been obtained by solving the following 2D Poisson's equations in cylindrical co-ordinate system [25],

$$\frac{\partial^2\phi_i(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial^2\phi_i(r,z)}{\partial r^2}+\frac{\partial^2\phi_i(r,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{Si}} \tag{0.1}$$

The subscript i = 1, 2 and 3 are used for channel region I, II and III respectively. It should be noted that q is the electronic charge; ε_{Si} is the permittivity of the Si film. The potential distributions in all the three regions are approximated by a parabolic polynomial as

$$\phi_i(r,z)=C_{0i}(z)+C_{1i}(z)r+C_{2i}(z)r^2 \tag{0.2}$$

The coefficients C_{0i}, C_{1i} and C_{2i} are the functions of z only, and can be determined by following the given boundary conditions.

The continuity of potential and electric field across the interface of the three regions are:

$$\phi_1(r,L_1)=\phi_2(r,L_1) \tag{0.3}$$

$$\left[\frac{\partial\phi_1(r,z)}{\partial z}\right]_{z=L_1}=\left[\frac{\partial\phi_2(r,z)}{\partial z}\right]_{z=L_1} \tag{0.4}$$

$$\phi_2(r,L_1+L_2)=\phi_3(r,L_1+L_2) \tag{0.5}$$

$$\left[\frac{\partial\phi_2(r,z)}{\partial z}\right]_{z=L_1+L_2}=\left[\frac{\partial\phi_3(r,z)}{\partial z}\right]_{z=L_1+L_2} \tag{0.6}$$

The continuity of electric flux across the SiO_2/Si interface under all the three gate metals [23] is given as:

$$\left[\frac{\partial\phi_i(r,z)}{\partial r}\right]_{z=\frac{t_{Si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_{GS}-V_{fbi}-\phi_i\left(\frac{t_{Si}}{2},z\right)}{t'_{ox}} \tag{0.7}$$

where,

$$t'_{ox} = \frac{t_{Si}}{2}\ln\left(1+\frac{2t_{ox}}{t_{Si}}\right) \tag{0.8}$$

and ε_{ox} is the permittivity of the SiO_2, t'_{ox} is the effective oxide thickness, t_{ox} is the thickness of gate oxide. V_{GS} denotes the gate to source voltage, V_{fbi} are the channel flat-band voltages of Si film given by

$$V_{fbi} = \varphi_{Mi} - \phi_w, i = 1,2,3 \tag{0.9}$$

$$\text{where, } \phi_w = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{0.10}$$

φ_{Mi} represents the metal work functions above the regions 1,2 and 3; ϕ_w is silicon work-function.

Potentials at source-channel and drain-channel interfaces are, respectively, given by

$$\phi_1(r,0) = V_{bi} \tag{0.11}$$

and

$$\phi_1(r, L_1 + L_2 + L_3) = V_{bi} + V_{DS} \tag{0.12}$$

where, V_{bi} is the built-in voltage between the source/drain and Si channel junction and is given by

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{0.13}$$

and V_{DS} is drain-to-source voltage.

The potentials at the body centre, $\phi_{ci}(z)$, and at the surface, $\phi_{si}(z)$, are, respectively, given by

$$\phi_{ci}(z) = \phi_i(0,z) \tag{0.14}$$

and,

$$\phi_{si}(z) = \phi_i\left(\pm\frac{t_{Si}}{2}, z\right) \tag{0.15}$$

By utilizing Eqs. (4.11)- (4.12) in Eq. (4.2), the center potential and the surface potential can be related as

$$\phi_{ci}(z) = \phi_{si}(z)\left(1+\frac{\varepsilon_{ox}t_{Si}}{4\varepsilon_{Si}t'_{ox}}\right) - \frac{\varepsilon_{ox}t_{Si}}{4\varepsilon_{Si}t'_{ox}}\left(V_{GS} - V_{fbi}\right) \tag{0.16}$$

Solving Eq. (1) using Eq.(2) and the boundary conditions described from Eqs.(3) to (16) gives the following one-dimensional differential equation of the centre potential, $\phi_{ci}(z)$,

$$\frac{\partial^2\phi_{ci}(z)}{\partial z^2} - \frac{1}{\lambda_c{}^2}\phi_{ci}(z) = D_{ci} \tag{0.17}$$

where, $\lambda_c = \sqrt{\dfrac{2\varepsilon_{Si}t_{Si}^2\ln\left(1+\dfrac{2t_{ox}}{t_{Si}}\right)+\varepsilon_{ox}t_{Si}^2}{16\varepsilon_{ox}}}$ (0.18)

is characteristic length and

$$D_{c_i} = \frac{qN_a}{\varepsilon_{si}} - \frac{1}{\lambda_c{}^2}(V_{GS} - V_{fbi}) \tag{0.19}$$

Utilizing Eqs. (4.6), (4.8), (4.14) and (4.15) for solving Eq. (4.17), gives central channel potential, $\phi_{ci}(z)$, as

$$\phi_{c1}(z) = \frac{(V_{p1}+\sigma_1)\sinh\left(\dfrac{z}{\lambda_c}\right) - (V_{bi}+\sigma_1)\sinh\left(\dfrac{z-L_1}{\lambda_c}\right)}{\sinh\left(\dfrac{L_1}{\lambda_c}\right)} - \sigma_1 \tag{0.20}$$

$$\phi_{c2}(z)=\frac{(V_{p2}+\sigma_2)\sinh\left(\frac{z-L_1}{\lambda_c}\right)-(V_{p1}+\sigma_2)\sinh\left(\frac{z-L_1-L_2}{\lambda_c}\right)}{\sinh\left(\frac{L_2}{\lambda_c}\right)}-\sigma_2 \tag{0.21}$$

and

$$\phi_{c3}(z)=\frac{(V_{bi}+V_{DS}+\sigma_3)\sinh\left(\frac{z-L_1-L_2}{\lambda_c}\right)-(V_{p2}+\sigma_3)\sinh\left(\frac{z-L_1-L_2-L_3}{\lambda_c}\right)}{\sinh\left(\frac{L_3}{\lambda_c}\right)}-\sigma_3 \tag{0.22}$$

where, $\sigma_i=\lambda_c^2 D_{ci}$ (0.23)

V_{p1} is assumed as the interface potential between regions 1 and 2 given by

$$V_{p1}=\frac{b_2c_1-b_1c_2}{a_1b_2-a_2b_1} \tag{0.24}$$

And, V_{p2} is assumed the interface potential between regions 2 and 3 and given by

$$V_{p2}=\frac{a_2c_1-a_1c_2}{a_1b_2-a_2b_1} \tag{0.25}$$

where, $a_1=\coth\left(\frac{L_1}{\lambda_c}\right)+\coth\left(\frac{L_2}{\lambda_c}\right)$ (0.26)

$$b_1=-\cos ech\left(\frac{L_2}{\lambda_c}\right) \tag{0.27}$$

$$c_1=V_{bi}\cos ech\left(\frac{L_1}{\lambda_c}\right)+\sigma_2\left(\cos ech\left(\frac{L_2}{\lambda_c}\right)-\coth\left(\frac{L_2}{\lambda_c}\right)\right)+\sigma_1\left(\cos ech\left(\frac{L_1}{\lambda_c}\right)-\coth\left(\frac{L_1}{\lambda_c}\right)\right)$$
(0.28)

$$a_2=-\cos ech\left(\frac{L_2}{\lambda_c}\right) \tag{0.29}$$

$$b_2=\coth\left(\frac{L_2}{\lambda_c}\right)+\coth\left(\frac{L_3}{\lambda_c}\right) \tag{0.30}$$

$$c_2=(V_{bi}+V_{DS})\cos ech\left(\frac{L_3}{\lambda_c}\right)+\sigma_2\left(\cos ech\left(\frac{L_2}{\lambda_c}\right)-\coth\left(\frac{L_2}{\lambda_c}\right)\right)+\sigma_3\left(\cos ech\left(\frac{L_3}{\lambda_c}\right)-\coth\left(\frac{L_3}{\lambda_c}\right)\right) \tag{0.31}$$

It should be noted that the minimum of central potential, $\phi_{ci,\min}$, lies in region I due to the fact that metal gate with highest work function surrounds channel region I. The position , $z_{\min}$, of the minimum surface potential, $\phi_{ci,\min}$, can be determined by solving $\frac{d\phi_{c1}}{dz} = 0$ and is given as

$$z_{\min} = \frac{\lambda_c}{2} \ln\left(\frac{B_1}{A_1}\right) \tag{0.32}$$

where, $$A_1 = -\frac{e^{-\frac{L_1}{\lambda_c}}(V_{bi}+\sigma_1) - (V_{p1}+\sigma_1)}{2\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.33}$$

$$B_1 = \frac{e^{\frac{L_1}{\lambda_c}}(V_{bi}+\sigma_1) - (V_{p1}+\sigma_1)}{2\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.34}$$

By substituting the values of the minima position into Eq. (4.20), the minimum surface potential can be expressed

$$\phi_{c1,\min} = 2\sqrt{A_1 B_1} - \sigma_1 \tag{0.35}$$

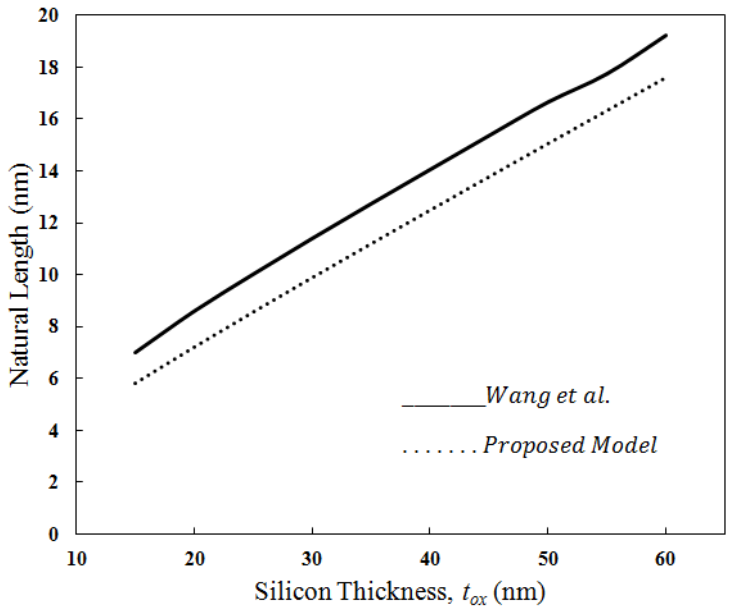


Fig. 0.1 Comparison of the natural length for **[23]** and the proposed model against Silicon thickness.

The

characteristic lengths of the surface potential of [23] and the centre potential of proposed

model are compared in Fig. 4.1 for silicon channel thickness variation. It should be noted that model of [23] utilizes the surface potential for threshold voltage modeling. The result shows that the natural length associated with the proposed centre potential model is smaller than the natural length estimated by [23]. This concludes that the model of [23] is not estimating the accurate value of threshold voltage and hence the structure can be scaled down to the lower dimensions beyond the expectation of the [23].

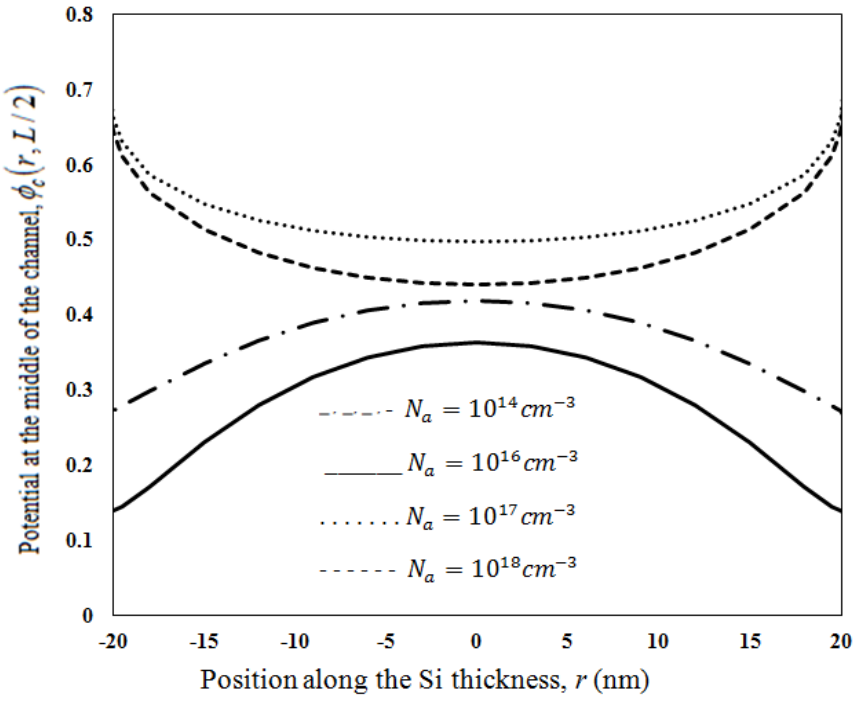


Fig. 0.2 The Electrostatic potential along the Si thickness and at the channel middle at different doping concentrations.

The simulation is carried out by Sentauras, a 3-D numerical simulator from Synopsis Inc [24]. Fig. 4.2 shows the potential variation along the Si thickness at the middle of the channel. The potential curves are plotted for different channel doping concentrations, N_a. It is observed that for an undoped channel, the potential maxima and hence the inversion charges are formed at the body center of the cylinder. On the other hand, for a doped channel, the potential is maximum at the Si/SiO_2 interface. This observation conform the use of center

potential model as appropriate choice over the surface potential model for developing the threshold model for an undoped TM-SGAA MOSFET.

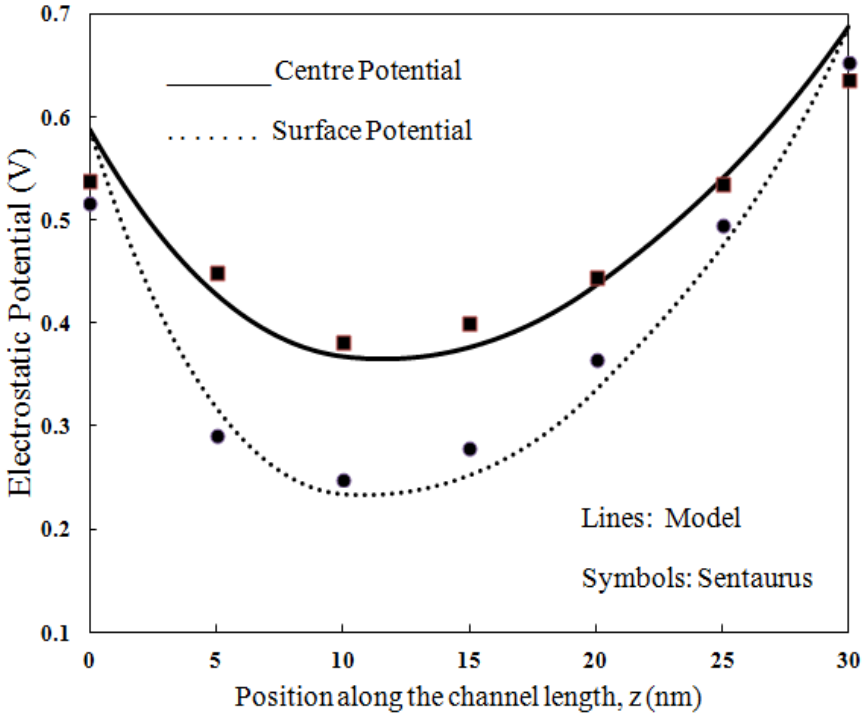


Fig. 0.3 The Potential versus the channel length at the body centre and at the surface. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3}=4.4*eV*, $N_a = 10^{16} cm^{-3}$, t_{Si}=40*nm*, L=30*nm*, L_1:L_2:L_3=1:1:1, t_{ox}=2*nm*, V_{GS}=0.1*V*, V_{DS}=0.1*V*

The centre potential, ϕ_c , and the surface potential, ϕ_s , are compared in Fig. 4.4. The surface potential curve lies below the centre potential one along with their minimum potential points. It is observed that source channel barrier height at channel centre is lower than that at the surface and hence threshold voltage should be determined by centre potential in contrast to [23].

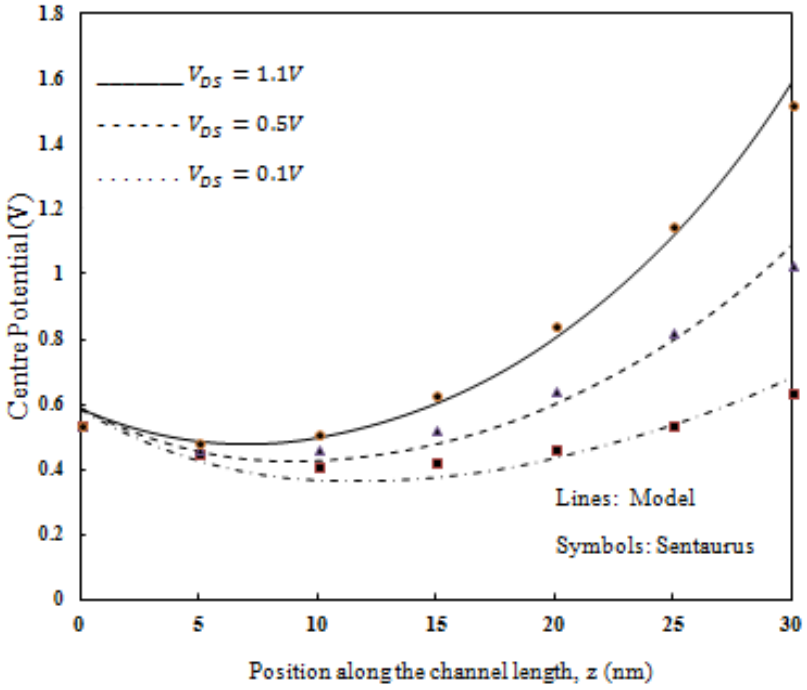


Fig. 0.4. The Centre Potential versus the channel length at various drain voltages. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV φ_{M3} = 4.4eV, $N_a = 10^{16} cm^{-3}$, L = 30nm, L_1:L_2:L_3=1:1:1, t_{ox}=2*nm*,t_{Si}=40*nm*, V_{GS}=0.1*V*

Fig. 4.4 shows the centre potential curve along the channel length at various values of the drain voltage. The minimum potential point shows a upward movement with the increasing drain voltage. This shift in the minimum potential value with changing drain voltage shows the presence of the DIBL effect.

Fig. 4.5 shows the centre potential curve along the channel length for different gate length ratio, L_1:L_2:L_3. It is seen that as the length of the screen gates increases, the magnitude of the minimum potential point rises with a shift towards the source side. It can be predicted that the DIBL reduces as screen gate length increases which is due to the shift in the minimum potential point away from the drain. But at the same time, other short channel effects rises due to the lesser control gate length and its lesser control over the channel.

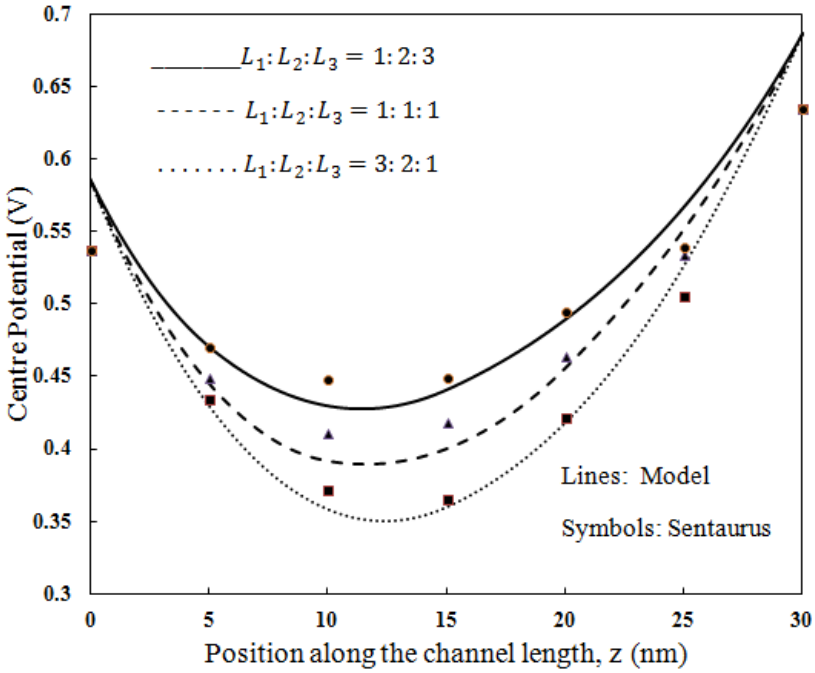


Fig. 0.5. The Centre Potential versus the channel length at various gate length ratios $L_1 : L_2 : L_3$. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L = 30nm, t_{ox} = 2nm, t_{Si} = 40nm, V_{GS} = 0.1V, V_{DS} = 0.1V

4.2. Threshold Voltage and DIBL Formulation

The threshold voltage V_{th} can be found as follows [23]:

$$\phi_{c1\min}\Big|_{V_{GS}=V_{th}} = 2\phi_{F,Si} = \phi_{th} \tag{0.36}$$

$$\phi_{F,Si} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{0.37}$$

where, $\phi_{F,Si}$ is the difference between the Fermi potential and the intrinsic Fermi level in the bulk region, ϕ_{th} is the value of central potential at which the volumetric inversion electron charge density in the Si device is equal to the body doping.

Solving (4.36), we obtain the final expression of threshold voltage as

$$V_{th} = \frac{-q-\sqrt{q^2-4pr}}{2p} \tag{0.38}$$

where,

$$p = 1 + v_1 v_2 \tag{0.39}$$

$$q = u_1 v_2 + u_2 v_1 - 2l \tag{0.40}$$

$$r = u_1 u_2 + l^2 \tag{0.41}$$

$$u_1 = \frac{(V_{bi} + s_1)\exp\left(-\frac{L_1}{\lambda_c}\right) - (V_{p11} + s_1)}{\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.42}$$

$$v_1 = \frac{1 - V_{p12} - \exp\left(-\frac{L_1}{\lambda_c}\right)}{\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.43}$$

$$u_2 = \frac{(V_{bi} + s_1)\exp\left(\frac{L_1}{\lambda_c}\right) - (V_{p11} + s_1)}{\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.44}$$

$$v_2 = \frac{1 - V_{p12} - \exp\left(\frac{L_1}{\lambda_c}\right)}{\sinh\left(\frac{L_1}{\lambda_c}\right)} \tag{0.45}$$

$$V_{p11} = \frac{b_2 c_{11} - b_1 c_{21}}{a_1 b_2 - a_2 b_1} \tag{0.46}$$

$$V_{p12} = \frac{b_2 c_{12} - b_1 c_{22}}{a_1 b_2 - a_2 b_1} \tag{0.47}$$

$$c_{11} = \left(\cos ech\left(\frac{L_2}{\lambda_c}\right) - \coth\left(\frac{L_2}{\lambda_c}\right)\right)s_2 + \left(\cos ech\left(\frac{L_1}{\lambda_c}\right) - \coth\left(\frac{L_1}{\lambda_c}\right)\right)s_1 + V_{bi}\cos ech\left(\frac{L_1}{\lambda_c}\right) \tag{0.48}$$

$$c_{12} = \coth\left(\frac{L_1}{\lambda_c}\right) + \coth\left(\frac{L_2}{\lambda_c}\right) - \cos ech\left(\frac{L_1}{\lambda_c}\right) - \cos ech\left(\frac{L_2}{\lambda_c}\right) \tag{0.49}$$

$$c_{21} = \left(\cos ech\left(\frac{L_2}{\lambda_c}\right) - \coth\left(\frac{L_2}{\lambda_c}\right)\right)s_2 + \left(\cos ech\left(\frac{L_3}{\lambda_c}\right) - \coth\left(\frac{L_3}{\lambda_c}\right)\right)s_3 + (V_{bi} + V_{DS})\cos ech\left(\frac{L_3}{\lambda_c}\right) \tag{0.50}$$

$$c_{12} = \coth\left(\frac{L_2}{\lambda_c}\right) + \coth\left(\frac{L_3}{\lambda_c}\right) - \cos ech\left(\frac{L_2}{\lambda_c}\right) - \cos ech\left(\frac{L_3}{\lambda_c}\right) \tag{0.51}$$

$$s_i = \frac{qN_a}{\varepsilon_{Si}} + V_{fbi}, i = 1,2,3 \tag{0.52}$$

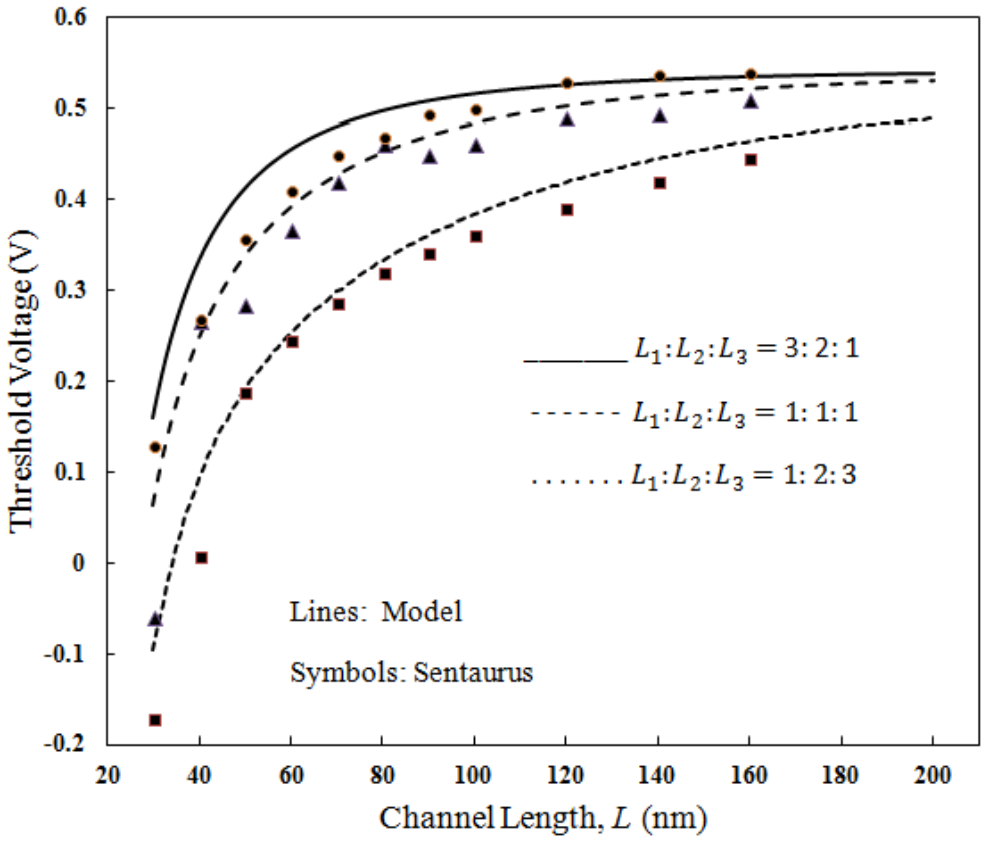


Fig. 0.6 . The linear threshold voltage versus channel length at different gate length ratio, $L_1 : L_2 : L_3$

Fig. 4.6 shows the threshold voltage versus channel lengths with different values of the gate length ratio in the linear region of device operation. It is observed that as the length of the screen gates increases, the threshold voltage decreases. This is due to the raise in the magnitude of the minimum centre potential point as discussed in the Fig. 4.5. Thus it may be established that longer screen gates reduces the HCE and DIBL but increases other SCEs.

Fig. 4.7 shows the threshold voltage versus channel lengths with different values of the gate length ratio ($L_1 : L_2 : L_3$) in the saturation region of device operation. The nature of the curves remains the same as in Fig. 4.6. The only difference lies in the decrease of the magnitude of the at the shorter channel lengths (say $L < 60nm$).

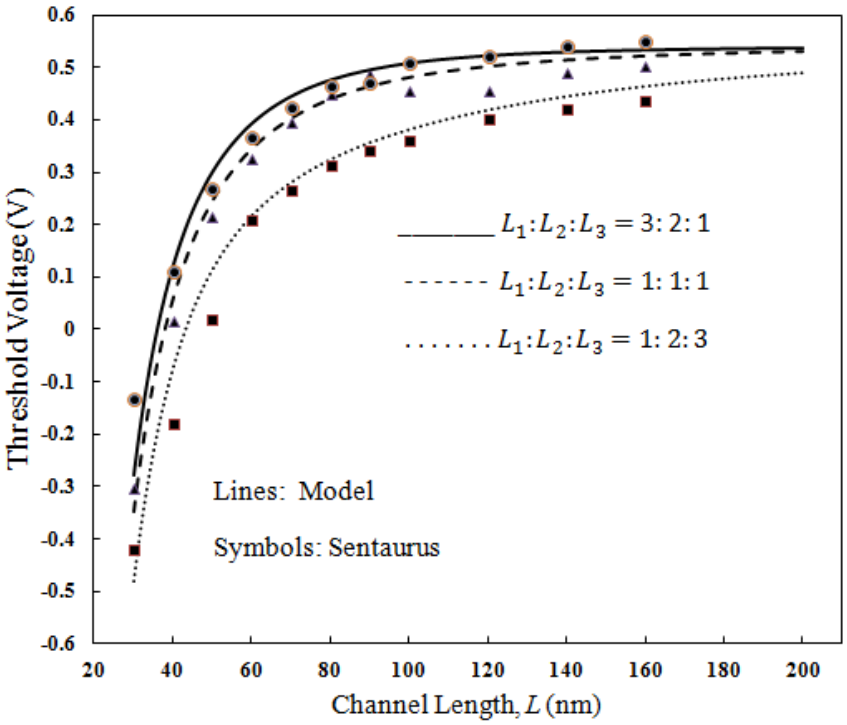
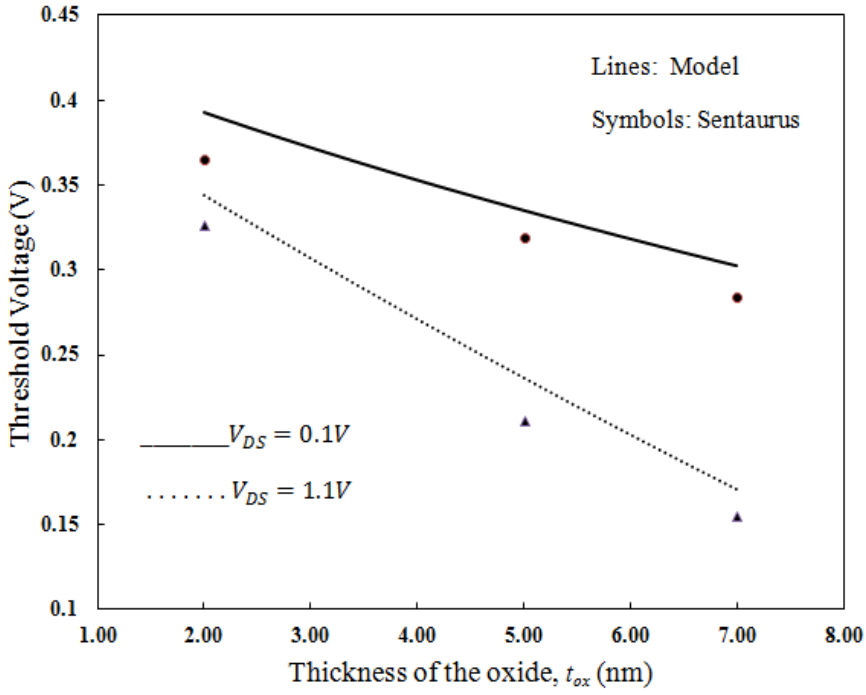


Fig. 0.8. The saturation threshold voltage versus channel length at different gate length ratio. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L = 30nm, t_{ox} = 2nm, t_{Si} = 40nm, V_{GS} = 0.1V, V_{DS} = 0.1V



0.9. The linear and saturation threshold voltage versus the gate oxide thickness. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, L_1:L_2:L_3=1:1:1, t_{Si}=40nm, V_{GS}=0.1V

Fig.4.8 shows the linear and saturation region threshold voltage variation with the gate oxide thicknesses, t_{ox}. As observed, the threshold voltage falls almost linearly with the increasing oxide thickness. As the oxide thickness increases the gate control over the channel diminishes leading to increased SCEs. The threshold voltage falls rapidly for the saturation region than the linear region.

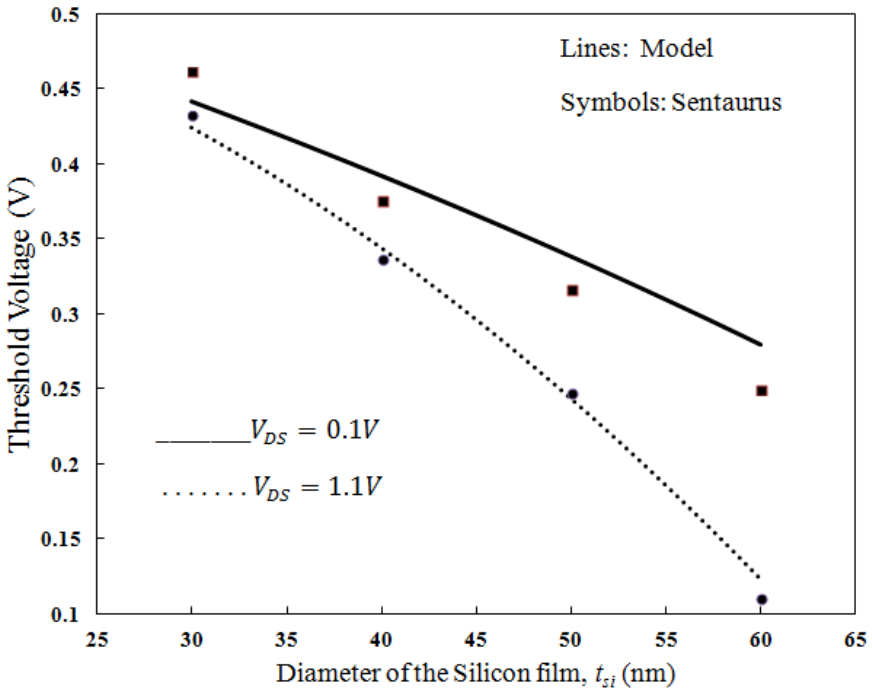


Fig. 0.10. The linear and saturation threshold voltage versus the Si film thickness. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, L_1:L_2:L_3=1:1:1,t_{ox}=2nm,V_{GS}=0.1V

Fig. 4.9 shows the linear and saturation region threshold voltage variation with the Si film thickness, t_{Si}. As observed, the threshold voltage falls non-linearly with the increasing Si film thickness. This is due to lower value of ratio at higher channel thicknesses. The threshold voltage falls rapidly for the saturation region than the linear region. This shows the dominance of the drain voltage over the gate voltage at such a short channel length for increasing .

The DIBL for a short-channel TM-CGAA MOSFET is computed as [16]

$$DIBL = \frac{V_{th}\big|_{V_{DS}=0.1V} - V_{th}\big|_{V_{DS}=1.1V}}{(V_{DS}=1.1V)-(V_{DS}=0.1V)} \tag{0.53}$$

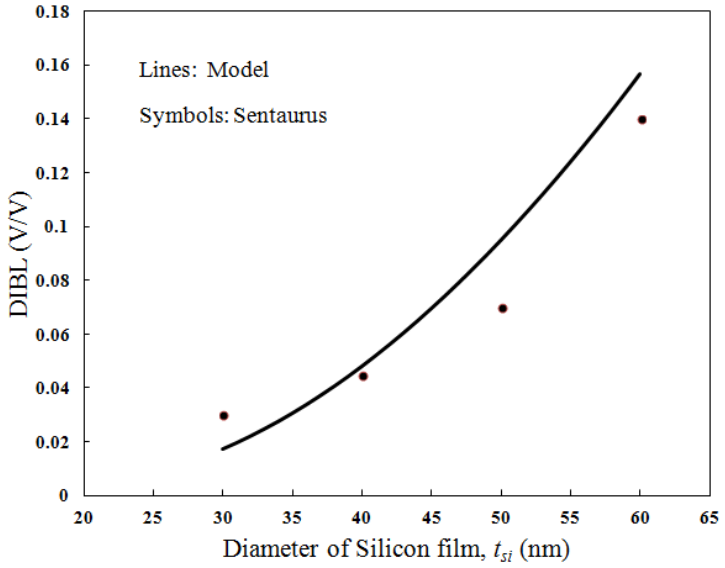


Fig. 0.11 . DIBL versus the Si thickness. Parameters used: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30*nm*, L_1:L_2:L_3=1:1:1,t_{ox}=2*nm*,V_{GS}=0.1*V*

Fig. 0.11 shows the DIBL variation with the Si film thicknesses. The DIBL increases non-linearly with the increase in Si channel thickness.

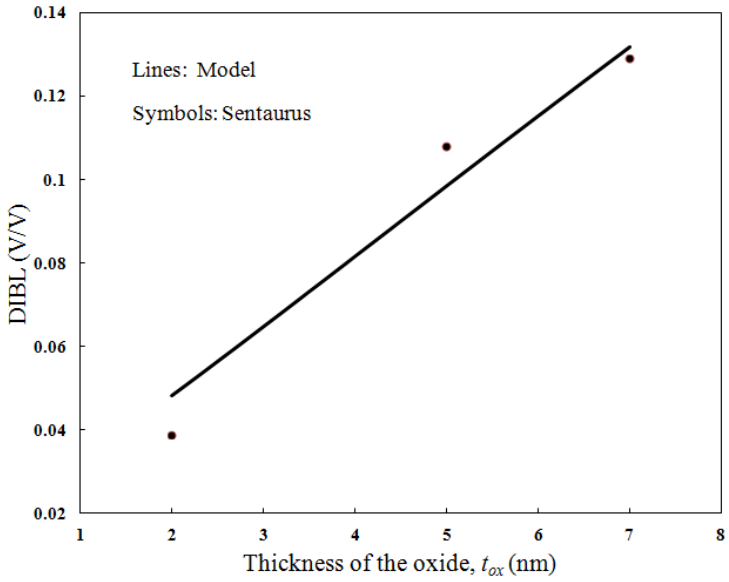


Fig. 0.13 DIBL versus channel length for different gate length ratio. Parameters used: φ_{M1} = 4.8eV,φ_{M2} = 4.6eV, φ_{M3} = *4.4eV*, *L* = *30nm*, t_{ox}= 2nm,t_{Si} = 40nm, V_{GS} = 0.1V

As the Si channel thickness increases, the gate loses its control over the channel carriers while the drain gains more control on the same leading to increased magnitude of DIBL.

Variation of DIBL against the gate oxide thickness is shown in Fig.12. The DIBL increases almost linearly with the oxide thickness. As the oxide thickness increases, the gate losses its control over the channel leading to increased control by the drain. So, the should be maintained optimum to avoid the DIBL effects.

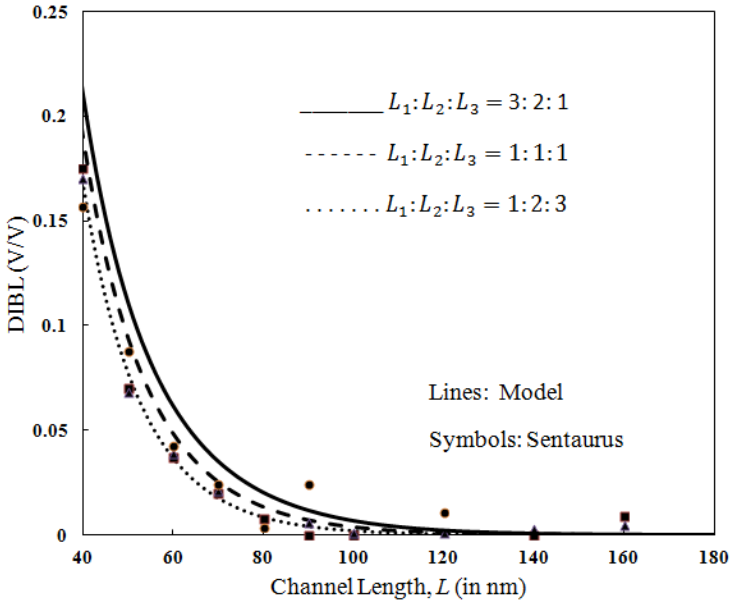


Fig. 0.14 DIBL versus the oxide thickness. φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, L_1:L_2:L_3=1:1:1,t_{Si}=40nm,V_{GS}=0.1V

Fig.13. shows the DIBL variation with the channel length for different gate length ratios. It is observed that the DIBL is negligible for longer channel lengths (above 120 nm), but is significant for smaller channel lengths (below 60–70 nm). The DIBL increases sharply as the length of the control gate increases. The reason being the shift of the minimum surface potential point towards the drain end, thereby increasing the drain influence on it. Thus, larger screen gate leads to lesser DIBL.

Chapter 5

SUB-THRESHOLD DRAIN CURRENT AND SUB-THRESHOLD SWING FORMULATION

5.1. Sub-Threshold Drain Current

Subthreshold leakage or subthreshold drain current is defined as a current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region of operation, that is, for gate-to-source voltages below the threshold voltage.

In literature a varied definition exists for subthreshold depending on the application. For a digital circuit, subthreshold conduction is considered as a parasitic *leakage* in a state that would ideally have no current. On the other hand, in micropower analog circuits, weak inversion is an efficient operating region, and subthreshold is a useful transistor mode around which circuit functions are designed [26].

In the past, the subthreshold conduction of transistors has been very small, but as transistors have been scaled down, leakage from all sources has increased. For a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption [27].

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. The amount of subthreshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device *off*, and as subthreshold conduction varies exponentially with gate voltage, it becomes more and more significant as MOSFETs shrink in size [28].

Subthreshold conduction is only one component of leakage: other leakage components that can be roughly equal in size depending on the device design are gate-oxide leakage and junction leakage.

The sub-threshold drain current may be formulated from [22] as

$$I_d = \frac{\mu_n \pi t_{Si}^2 n_i^2 KT\left(1-e^{\frac{-V_{DS}}{V_T}}\right)}{\int_0^L Q_j^{-1}(z)dz} = \frac{\mu_n \pi t_{Si}^2 n_i^2 KT\left(1-e^{\frac{-V_{DS}}{V_T}}\right)}{\int_0^{L_1} Q_1^{-1}(z)dz + \int_{L_1}^{L_1+L_2} Q_2^{-1}(z)dz + \int_{L_1+L_2}^{L_1+L_2+L_3} Q_3^{-1}(z)dz} \tag{0.1}$$

where, the depletion charges is given by, $Q_j(z) \approx \frac{t_{Si} q n_i^2 e^{\frac{\phi_{cj,\min}}{V_T}}}{2N_a}$, j=1,2,3 (0.2)

Solving Eq. (5.1) with (5.2), the following expression is achieved

$$I_d = \frac{\mu_n \pi t_{Si}^2 n_i^2 KT\left(1-e^{\frac{-V_{DS}}{V_T}}\right)}{\left(\frac{L_1}{e^{\frac{\phi_{c1,\min}}{V_T}}} + \frac{L_2}{e^{\frac{\phi_{c2,\min}}{V_T}}} + \frac{L_3}{e^{\frac{\phi_{c3,\min}}{V_T}}}\right) N_a} \tag{0.3}$$

Since $\phi_{c3,\min} > \phi_{c2,\min} > \phi_{c1,\min}$, the above expression may be reduced as

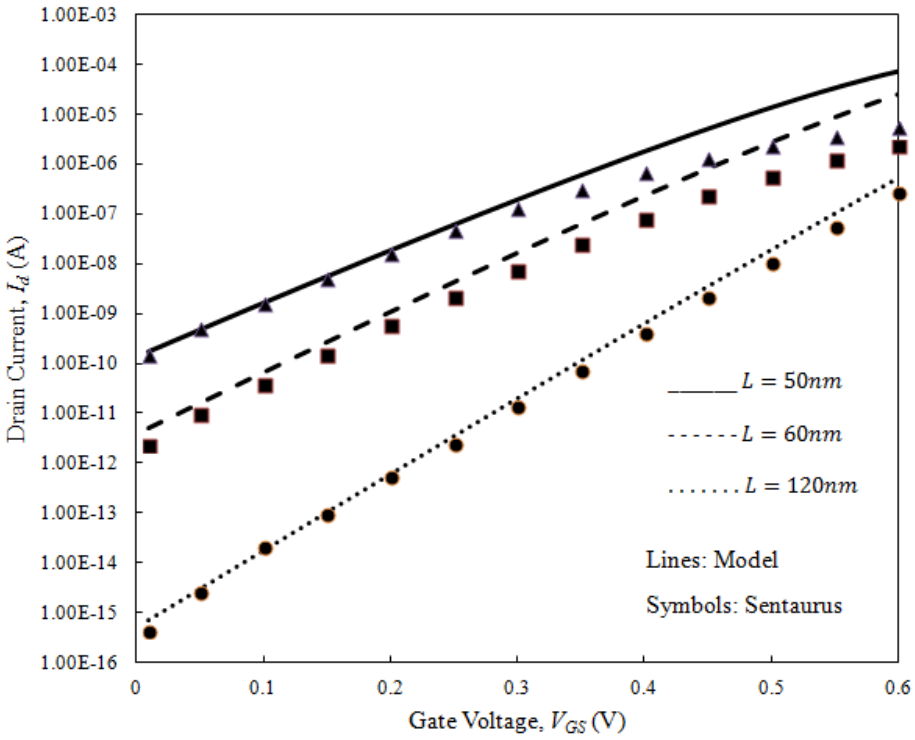
$$I_d \approx \frac{\mu_n \pi t_{Si}^2 n_i^2 KT\left(1-e^{\frac{-V_{DS}}{V_T}}\right) e^{\frac{\phi_{c1,\min}}{V_T}}}{L_1 N_a} \tag{0.4}$$

From the above expression, it may be concluded that, I_d is

1. directly proportional to the exponent of minimum centre potential,
2. directly proportional to V_{DS} (obtained by series expansion of $e^{\frac{-V_{DS}}{V_T}}$),
3. directly proportional to t_{Si}^2, and

4. inversely proportional to L_1.

These relations are further verified through the simulations as shown in the following plots.



0.1. . Dependence of subthreshold current on gate bias for different channel lengths. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, $\mu_n = 1076cm^2/(V-s)$, $L_1{:}L_2{:}L_3$=1:1:1, t_{ox}=2nm,t_{Si}=40nm, V_{GS}=0.1V

Fig. 5.1 explores the length variations of the subthreshold drain current, I_d with the bias gate voltage V_{GS}. Since the minimum channel potential, $\phi_{c1,\min}$, is depended directly on the V_{GS}. Further, the exponential dependence of the $\phi_{c1,\min}$ bring orders of variation in the drain current. Now, for a given gate bias, the subthreshold drain current is lower for a longer channel length. This follows from the fact that the minimum channel potential, $\phi_{c1,\min}$ rises significantly with shorter channel lengths due to SCEs. Being exponential dependence of the drain current on the $\phi_{c1,\min}$, shorter channel lengths increases the subthreshold leakage significantly.

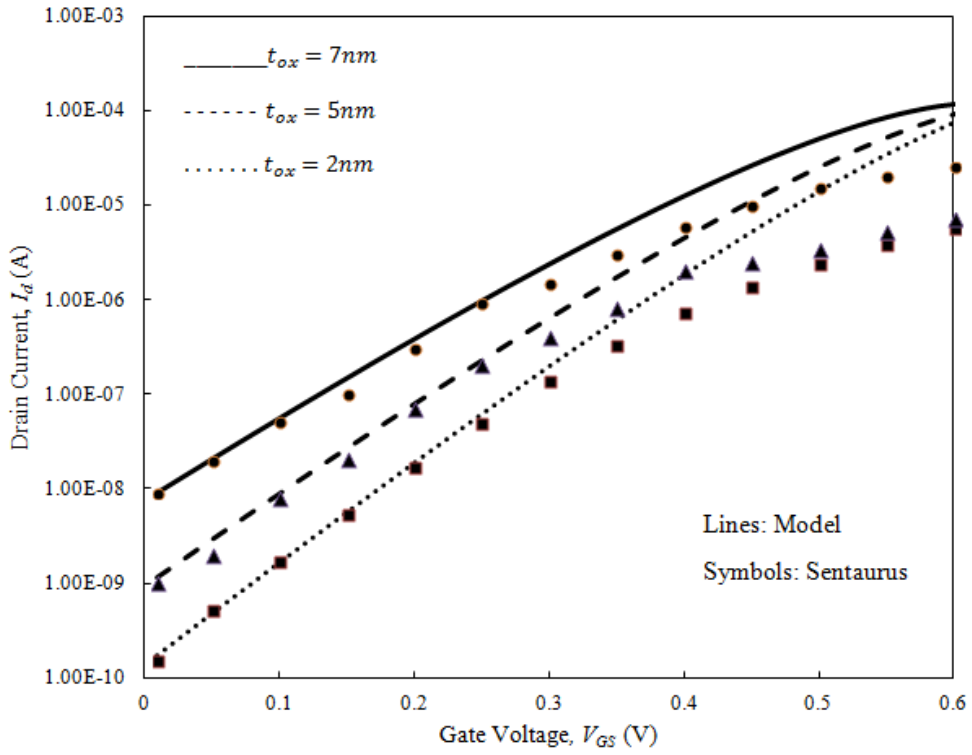


Fig. 0.2. Dependence of subthreshold current on gate bias for different gate oxide thickness. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, $\mu_n = 1076 cm^2/(V-s)$, L=60nm, L_1:L_2:L_3=1:1:1, t_{Si}=40nm, V_{GS}=0.1V

The oxide thickness dependence on the subthreshold drain current is analyzed in Fig. 5.2. The graph shows a lower subthreshold leakage for a thinner oxide thickness. For the instance, the drain current reduces by an order when a thinner oxide is used, from 7nm to 5nm or from 5nm to 2nm. This may be attributed to the greater gate control and lower SCEs at thinner gate oxide.

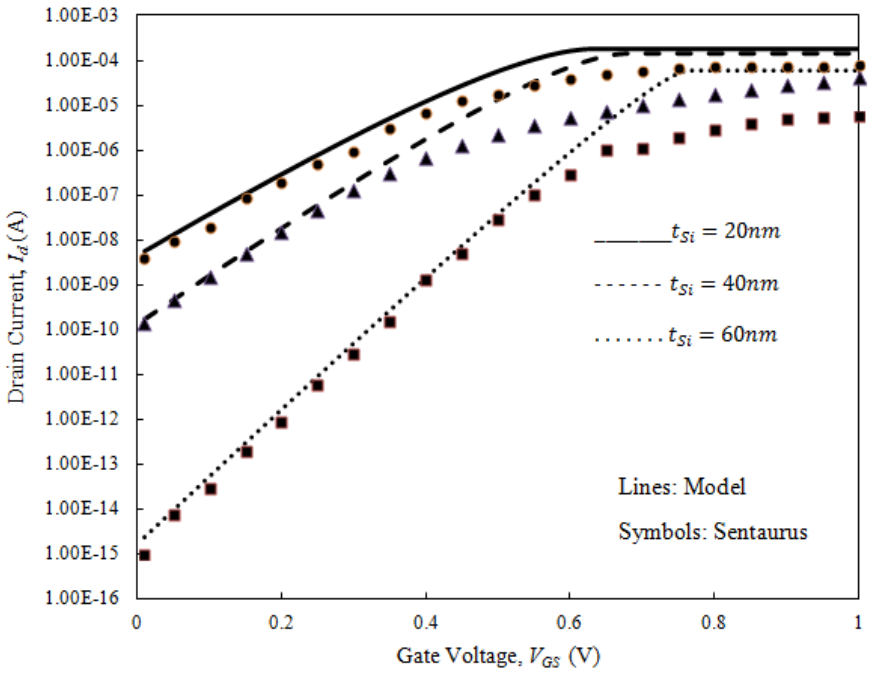


Fig.0.3. Dependence of subthreshold current on gate bias for different Silicon film thickness. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, $\mu_n = 1076 cm^2/(V-s)$, L=60nm, L_1:L_2:L_3=1:1:1, t_{Si}=40nm, V_{GS}=0.1V

Fig. 5.3 displays the silicon thickness dependence on the subthreshold drain current. As expected from the drain current expression of Eq. (), the drain current magnitude varies as the square of the silicon thickness. Thus, a thicker Si film will be suitable for a lower static power application.

The subthreshold current dependence on the control to screen gate ratio is manifested in the Fig. 5.4. For a lower L_1:L_2:L_3, the minimum centre potential rises leading to higher drain current in the subthreshold. Thus, a higher L_1:L_2:L_3 is intended to lower static power dissipation.

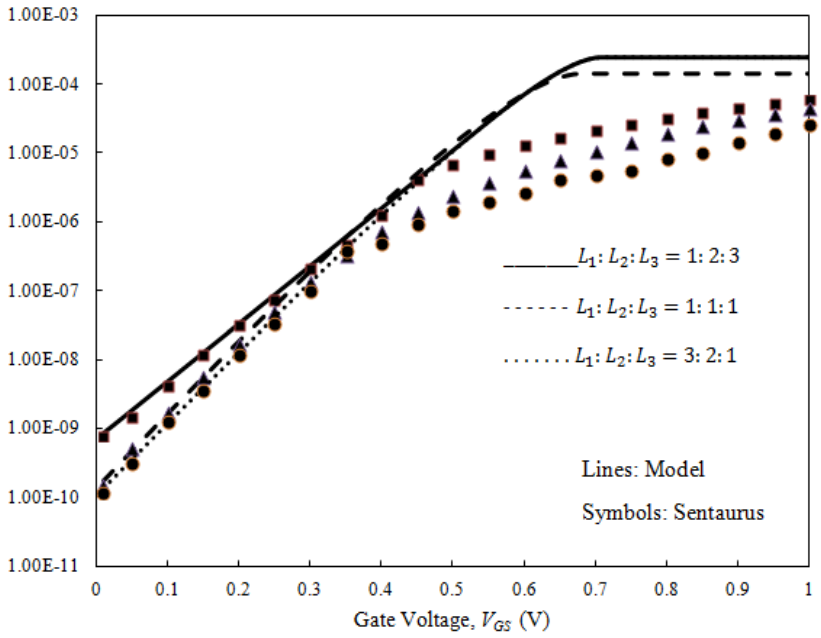


Fig.0.4. Dependence of subthreshold current on gate bias for different Control to screen gate ratio. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, $\mu_n = 1076 cm^2/(V-s)$, L=60nm, t_{Si}=40nm, V_{GS}=0.1V

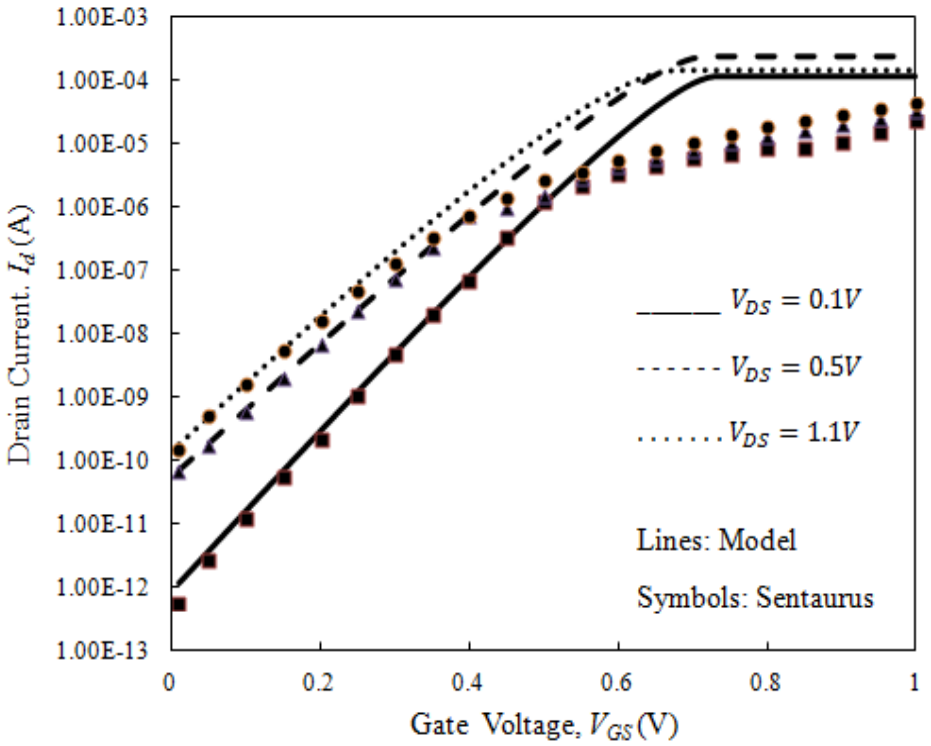


Fig.0.5. Dependence of subthreshold current on gate bias for different gate oxide thickness. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, $\mu_n = 1076 cm^2/(V-s)$, L=60nm, L_1:L_2:L_3=1:1:1, t_{Si}=40nm, V_{GS}=0.1V

The dependence of the subthreshold current on the drain voltage is plotted in Fig. 18. Increase in the drain voltage shifts up the minimum centre potential point which further exponentially increases the drain voltage.

5.1 Sub-Threshold Swing

The subthreshold swing is a subthreshold feature of a MOSFET's current-voltage characteristic. In the subthreshold region the drain current behaviour, though being controlled by the gate terminal is similar to the exponentially increasing current of a forward biased diode. Therefore a plot of logarithmic drain current versus gate voltage with drain, source, and bulk voltages fixed will exhibit approximately linear behaviour in this MOSFET operating regime. In short it is the inverse slope of subthreshold drain curren. A device characterized by steep subthreshold slope exhibits a faster transition between off (low current) and on (high current) states. It is a figure of demerit exhibiting SCEs.

The sub-threshold swing of a MOSFET is defined as [22],

$$S_t = \left(\frac{\partial V_{GS}}{\partial \log(I_d)} \right) \tag{0.6}$$

An approximate solution of the integral (5.7) given as,

$$S_t \approx V_T \ln(10) \left(\frac{\partial \phi_{s1,\min}}{\partial V_{GS}} \right)^{-1} \tag{0.7}$$

Therefore, a closed form expression for subthreshold swing for the CGAA MOSFET is

$$S_t \approx V_T \ln(10) \left(1 - \frac{1}{\sqrt{A_1 B_1}} \left[v_1 (u_2 + v_2 V_{GS}) + v_2 (u_1 + v_1 V_{GS}) \right] \right) \tag{0.8}$$

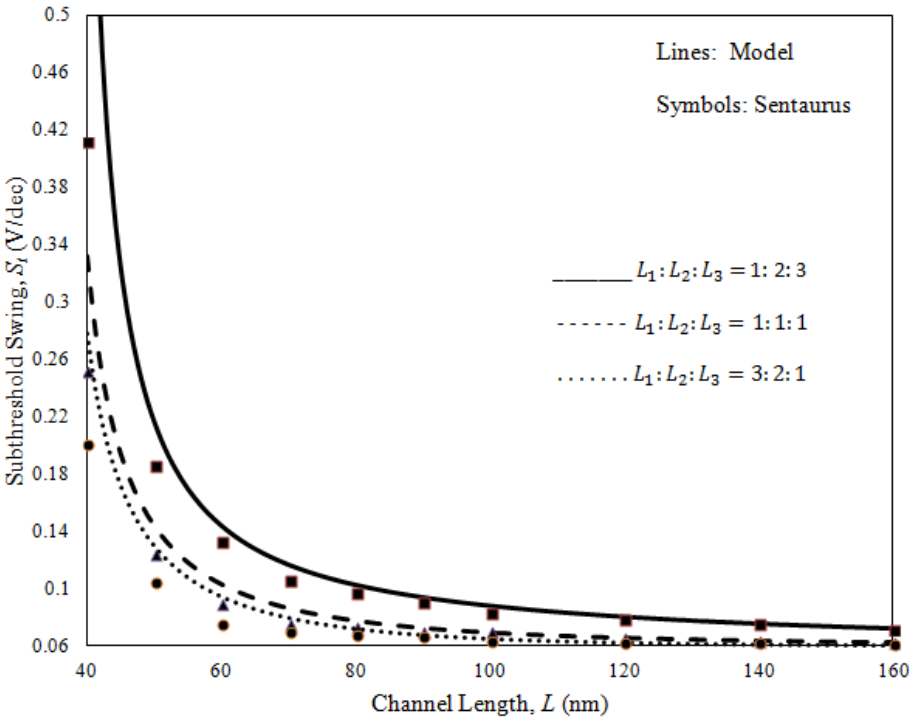


Fig.0.9. Subthreshold Swing versus channel length at different gate length ratio. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, t_{ox}=2nm,t_{Si}=40nm, V_{GS}=0.1V

Fig. 5.9 shows a Subthreshold Swing, S_t, variation against channel length for different gate length ratio. The swing increases incredibly at the lower channel for a lower L_1: L_2: L_3 ratio. For a lower control to screen gate ratio, the control gate loses control over the channel leading to increased SCEs as evident from higher magnitude of S_t.

Subthreshold Swing, S_t, variation with Silicon thickness variation is depicted in Fig. 5.10. The swing increases non-linearly with the Silicon thickness conforming rising SCEs. For a thicker Si film, the gate exerts lower control over the centre channel leading to increase in magnitude of S_t.

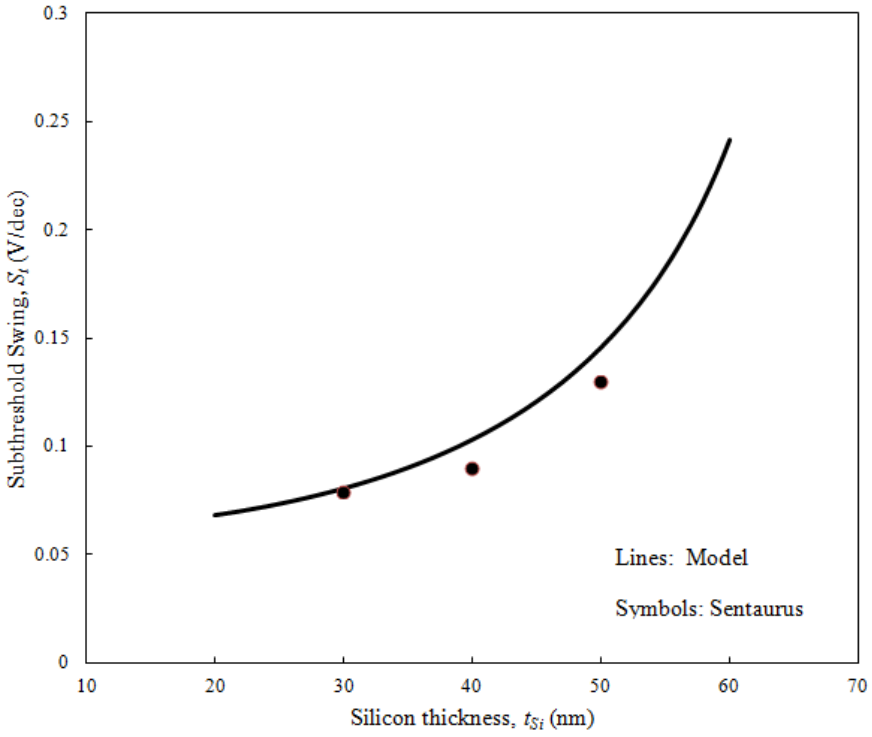


Fig. 0.10. Subthreshold Swing versus Silicon thickness. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, t_{ox}=2nm,t_{Si}=40nm, V_{GS}=0.1V

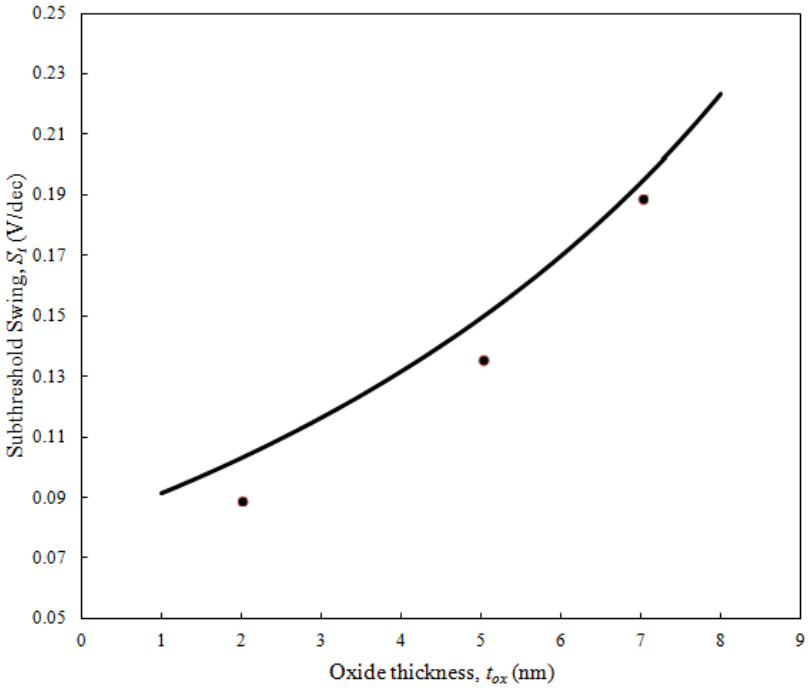


Fig.0.11. Subthreshold Swing versus gate oxide thickness. Parameters used are: φ_{M1} = 4.8eV, φ_{M2} = 4.6eV, φ_{M3} = 4.4eV, L=30nm, t_{ox}=2nm,t_{Si}=40nm, V_{GS}=0.1V

Subthreshold Swing, S_t, variation with the gate oxide thickness is depicted in Fig. 5.11. The swing increases non-linearly with the oxide thickness demonstrating rise in the SCEs. For a thicker oxide layer, the gate exerts lower control over the centre channel leading to increase in magnitude of S_t.

CONCLUSION

6.1. The Outcome

The work proposes an accurate subthreshold model for the TM-CGAA MOSFET considering a prior body inversion than the surface, which is demonstrated through simulations. A 2-D potential profile is derived by solving the 2-D Poisson's equation in cylindrical co-ordinate using a parabolic approximation of the channel. The work further proposes the natural length selection using centre potential as opposed to the previous work wherein the natural length based on surface potential was adapted. From the derived centre potential model, a threshold voltage and a DIBL model is obtained which proved to be more accurate than the previous work. An extensive analysis is carried out to find the impact of numerous device parameters like the silicon thickness, oxide thickness, gate length ratio, etc. on the threshold voltage and the DIBL. Increasing the screen gate length reduces the HCE and the DIBL effects, but other SCEs increases due to higher threshold voltage roll off. Thus, a trade off may be achieved in the threshold voltage swing and DIBL by selecting an appropriate gate length ratio. Also, an appropriate selection of the oxide and the silicon thickness, gives an optimum threshold voltage and DIBL at a given channel length. Next, an analytical subthreshold drain current model is proposed considering diffusion transportation at subthreshold condition. At lower channel length and channel length ratio, the leakage current increases significantly which may be curtailed through lower oxide thickness. Thicker silicon body lowers the leakage current. The subthreshold swing is modelled from the derived centre potential model. The subthreshold swing may be controlled by increasing the gate oxide and gate length ratio and lowering silicon thickness. The derived 2-D analytical model is found to be in good agreement with the simulation results obtained from Sentaurus^{TM} from Synopsys. The developed model may prove to a useful tool to optimize the desired

performance of the device parameters. These developed models may be incorporated in a circuit simulator for further VLSI design.

6.2. Scope for Future Work

The work may be extended to cover a detailed analysis of the device to explore its analog and digital characteristics.

The super-threshold parameters like drain current, transconductance, resistances, capacitances may be modeled for TM-CGAA. The procedure adopted may be to explore the Poisson's equation in the threshold and above regions including the effects of the mobile charges.

An extensive analysis of TM-CGAA may be carried out to obtain AC and frequency parameter models. AC gain, parasitic behavior may be modeled. The frequency analysis of the device will lead to finding cut-off frequency, oscillation frequency and maximum output frequencies.

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